DOLPHIN DESIGN

CHAMELEON

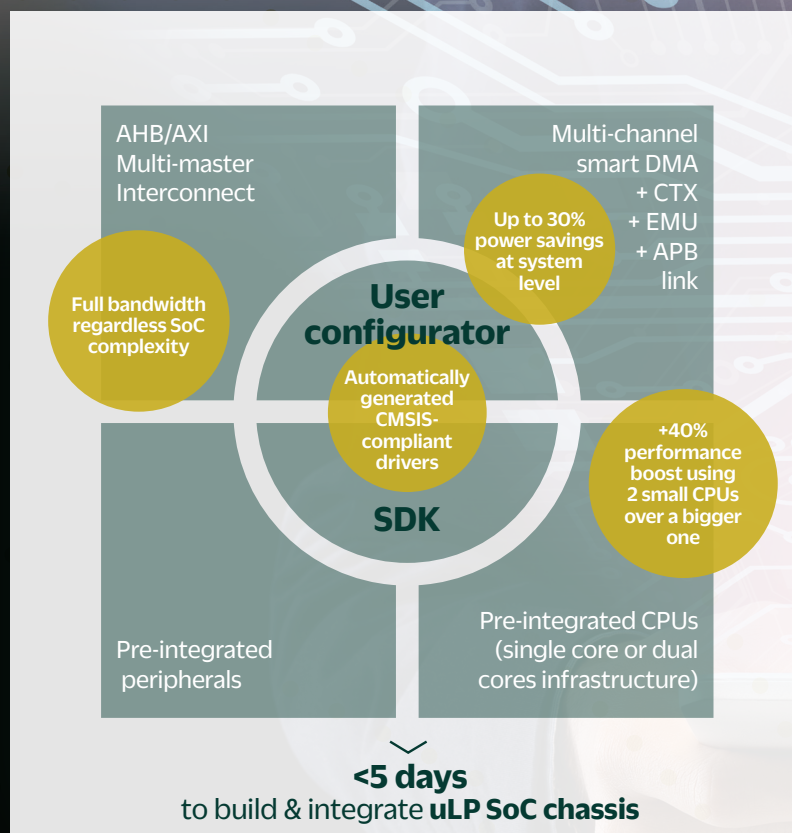# uLP SoC chassis IP platform

Open, user-configurable IP platform supporting CPUs from any vendor

Scalable AMBA-based chassis enabling maximum energy-efficiency for SoCs in days

AHB/AXI Multi-master Interconnect

Multi-channel smart DMA + CTX + EMU + APB link

Up to 30% power savings at system level

Full bandwidth regardless SoC complexity

User configurator

Automatically generated CMSIS-compliant drivers

+40% performance boost using 2 small CPUs over a bigger one

SDK

Pre-integrated peripherals

Pre-integrated CPUs (single core or dual cores infrastructure)

<5 days
to build & integrate **uLP SoC chassis**

Cost-effective approach to achieving ultimate energy efficiency with minimal risk

Off-the-shelf with silicon proven IP

Pick a part or go turnkey

Automated personalization

Ultimate energy efficiency

Chameleon IP design platform

CONFIGURABLE RTL IP

CPU 1

CPU 2
optionnal

CPU + debug stub (dual core)

CPU + debug stub (single core)

Multi-channel Smart DMA

Even Unit Manager

Context restorer

APB bridge

sDMA bridge

UART	GPIO
WDT	QSPI

...

Multi-master interleaved XBAR

AXI   AXI   AHB

SRAM	NPU	DSP	Connectivity

IP PLATFORM DELIVERABLES

RTL & DRIVER CONFIGURATOR

VERIFICATION ENVIRONMENT

DOCUMENTATION

VIRTUAL PLATFORM

SDK

Chameleon   3rd party IP

1. Pre-integrated CPU core (ARM, RISC-V) single or dual core configurations and debugging

2. Smart data & peripheral management subsystem with autonomous operation of peripherals (CPU-less)

3. Built-in peripherals and expandable to 3rd-party peripherals

4. High bandwidth system interconnect with built-in interleaving engine

5. User-configurable with comprehensive set of deliverables

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