DOLPHIN

DESIGN

ENERGY-EFFICIENCY WITHOUT LIMITS

EDGE / VERY EDGE / NANO EDGE APPLICATIONS

SPEED

State-of-the-art modular & qualified **IPs**

IP-to-SoC design tools to streamline SoC design & verifications

Best Energy Efficiency — **Up to x10 x10 x 10**

Lowered System Costs — **Up to x10 cts saved**

Improved Time-To-Success — **Up to 12 months saved**

Lowered Risks — **First Pass Success**

SEMICONDUCTOR IPs as clusters

Granting best SoC EE

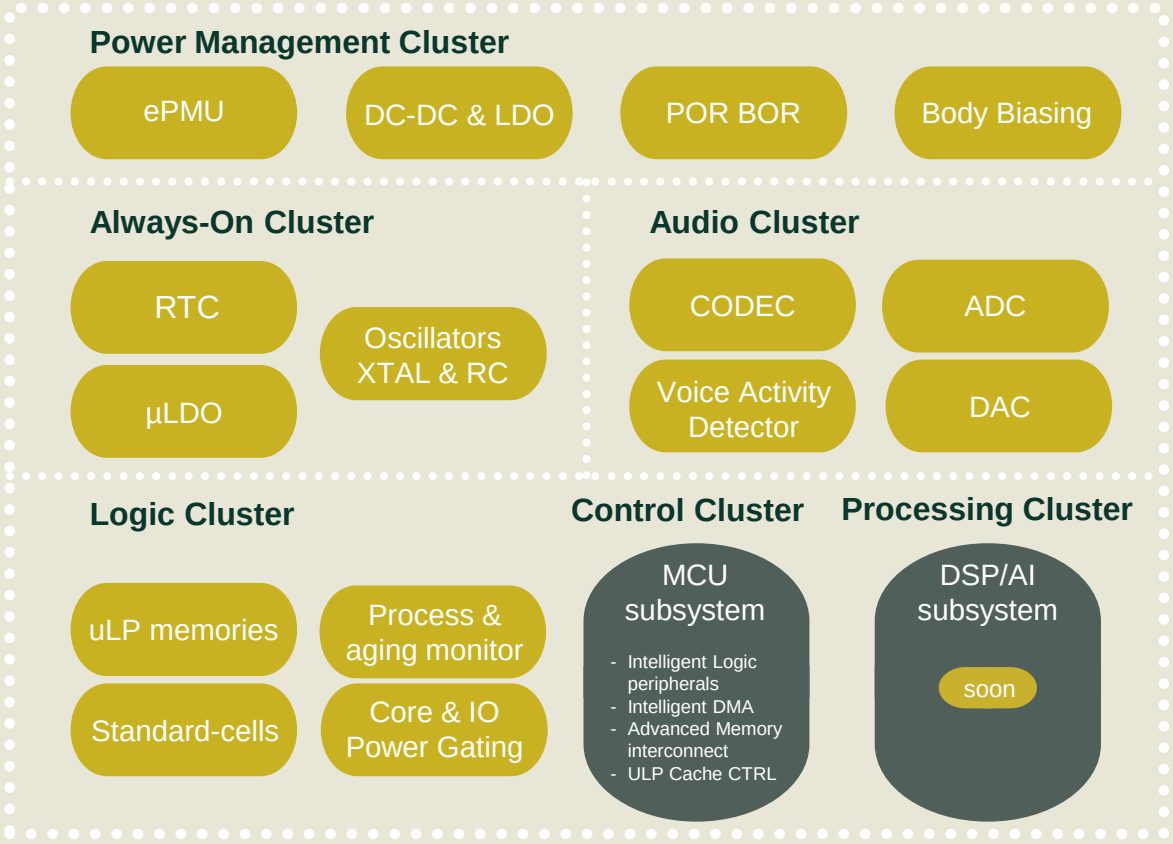
Down to **350 nA**
in sleep mode

Down to x**1 uA/MHz**
in active mode

In the range of **x10 uA**
in triggering mode

2 to 4 times faster mode
transitions

Configurable
RTL clusters



EE IPs TO DESIGN EE SoCs IN EACH POWER MODE

SLEEP MODE
Down to 350 nA

- uLDO incl. Vref: 140 nA
- POR-BOR-LP: 5 nA

- 32k RC Oscillator: 55 nA
- 32k XTAL Oscillator: 70 nA

- AON logic with thick oxide library: <20 nA

- Power gating of core domains: up to x10 leakage reduction

- IO power gating…

TRIGGERING MODE
In µA range

- Voice Activity Detector (always-on/DSP-less): 8 uA

- uLP comparator: 560 nA

- intelligent DMA: up to x3 lower power

- Intelligent peripherals (I2S…): up to x4 times lower power…

ACTIVE MODES
In µA/MHz range

- DC-DC converter: up to 95% efficiency with <5 mVpp switching noise

- Closed loop Adaptive Body Biasing for up to x10 EE improvement

- uLP audio ADC: 150 uA
- uLP audio DAC: < 1 mA

- uLP Cache Ctrl: up to x5 lower power…

MODE TRANSITIONS
x2 to x4 faster

- Combo VREG with continuous supply between sleep and active modes

- Up to x4 faster wake-up time of each power domain…

SPEED PLATFORMS: ENERGY-EFFICIENCY WITHOUT LIMITS

TURNKEY DESIGN SOLUTION

10x EE

POWER MANAGEMENT

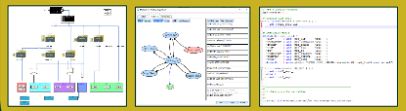
Power Management IP cluster

Complete library of proven power management IPs

VREG | PG | BB | Monitors | LS | OSC

IP-to-SoC Design Tool (PowerStudio™)

Selection and generation of best SoC power management architecture (RTL, testbench, UPF…)



10x & 10x EE

PROCESSING

MCU/DSP IP Clusters

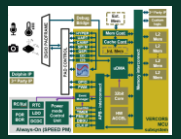
MCU subsystem incl. interface IPs, intelligent DMA, advanced memory interconnect…

DSP/AI subsystem incl. scalable DSP and AI cores with advanced memory interconnect

IP-to-SoC Design Tools

RTL & testbench configurator

Vercors
Event-based MCU subsystem



Chartreuse
DSP/AI processing system

Your PMU designed good by construction in 2 weeks

Push button generation of proven CPU architecture

Reduced design effort with reduced design risks