A Novel High-Voltage 5.5 V Resilient, Floating and Full-Scale 3.3 V Pulse-Triggered Level-Shifter

Nicolas Laflamme-Mayer and Mathieu Rnaud
Dolphin Integration, Jazz Department, Montreal, Canada

***Abstract*—This paper presents a novel 5.5 V resilient Pulse-Triggered-Level-Shifter (PTLS) with enhanced toggling speed. This PTLS is a based on a cascoded High-Voltage (HV) level-shifters and only uses 3.3 V, near minimum size, CMOS transistors. This HV level-shifter generates both floating and a full-scale output signals and is able to operate under supplies from 2.6 V (down to 1.8 V with strategic contextual gate control on cascode and protection transistors) up to 5.5 V, without endangering any transistors. This PTLS can drive pMOS logic, nMOS logic or 5.5 V I/Os simultaneously with loads up to 250 fF on every output nodes (1.25 pF total), using only one buffering stage. The proposed circuit was extensively validated by simulations for every technological corners, temperatures from -40 °C up to 125 °C, operating voltages and output capacitances, so that this HV level-shifter is reliable under any operating conditions. The simulated circuit shows a 2 39 ns maximum delay under typical conditions and a worst case of 10.4 ns. The circuit draws no static power and shows a typical dynamic power consumption of 25.92 µW/MHz with maximum operating frequency of 261.8 MHz.**

Keywords—Pulse-Triggered, Level-Shifter, high-voltage, HV, CMOS, fast, floating, full-scale, high speed, low-power, HVCMOS, HV CMOS, PTLS.

I. INTRODUCTION

Today's integrated circuits (ICs) ever increasing complexity and integration density tends to force the use of low-voltage (LV) nanometer CMOS technologies [1]. Indeed, optional tick oxide layers for HV transistors are not always available or convenient on a System-on-Chip (SoC) point of view. Many SoCs have to deal with only core and I/O devices (i.e. 1.8 V, 2.5 V and 3.3 V). On the other hand, the ever-growing demand from automotive, medical, MEMS, and portable electronics for efficient power management circuits such as DC-DC converters pushes towards the integration of the combined standard low-voltage (<3.63 V) and high-voltage (>3.63 V) supply rails on a single SoC [2]. Related examples can be found in portable applications (smart phones, MP3 players, GPS, etc) where autonomy has become pivotal. These portable systems often operate on lithium-ion batteries (4.2 V) and often need to be recharged by USB interface with 5.0 V ±10% (up to 5.5 V) supply while dealing with core transistor logic (0.9 V-1.2 V) and analog I/O (1.8 V, 2.5 V and 3.3 V). This implies new challenges to fully integrated LV and HV circuits into a low-voltage CMOS technology, where the maximum safe operating voltage is way below 5.5 V.

Level-shifters (LS) have increasingly become important modules, acting as interfaces between two different power-supply domains. There are two major types of level shifters: *the full-swing level-shifter and the floating level-shifter* [3]. Full-swing level-shifters translate from one power-supply to another and are typically used to drive output pins [2][4]. Floating level-shifters move the input signal to a different reference voltage, they are widely used to drive nMOS and pMOS transistors in high-voltage design applications [3]. The designs in [1], [3], [5]-[8] employ various floating level-shifter architectures with various performance results regarding, speed, static and dynamic power consumption, silicon area and maximum power supply. The present work will focus on floating level-shifters that draw no static current.

In [1], the authors proposed a level-shifter dedicated to control signals such as power-up, power-down, reset, enable, etc. Therefore, the speed of this design is suspected to be quite low as it is never specified. Both designs proposed in [3] and [5] offer good performances while remaining quite simple to implement. However, they require either HV CMOS technology or the use of Drain-extended MOS (DMOS): *high drain-source and drain-gate voltage but low gate-source voltage.* In [6], the authors used two differentially switch cascoded transistor ladders to offset the output signal by $2V_{DD}$ using a maximum power supply of $3V_{DD}$. However, the added cascoded transistors limit the minimum possible V_{DD} value. HV protection biasing is mandatory in a cascoded HV level-shifters, where these biasing voltages are usually applied on transistor gates draining no current. However, in [6] and [7] three different power supplies (V_{DD}, $2V_{DD}$ and $3V_{DD}$) are required where some are drain connected, powering various digital gates or high-voltage protection transistors. The designs in [8] and [9] display quiescent of 20 and 19 µA respectively. As a mean of fair comparison, the proposed design in this paper uses only 3.3 V transistors with no static power consumption. As for, only design using 3.3 V CMOS technology with no static power consumption will be discussed.

We present in this paper a HV tolerant level-shifter that only uses 3.3 V CMOS transistors. The proposed architecture is fast and was extensively validated for every technological process corners, temperatures (-40 °C to 125 °C) and its full input power supply capabilities up to 5.5 V. These validations were made in a 55 nm TSMC 3.3 V CMOS eFlash ultra low-power (uLP) technology. These validations are necessary to guaranty that the proposed level-shifter operates adequately within specifications in any cases. The rest of the paper is organized as follows. Section II describes the core circuit

limitations and its proposed ameliorations. Full circuit documentation is also presented in Section II, while Section III shows the simulation results that are discussed, and a conclusion closes this paper.

II. HV Tolerant Level-Shifter Implementation

A. Classic HV Level-Shifter Speed Limitations

The focus of this paper is aimed at designs that draw no static power and only uses standard 3.3 V transistors. A classic HV level-shifter can be seen in Fig. 1. This structure draws no static current and is high-voltage tolerant in the limits where transistors M1 to M8 gate-drain (V_{GD}), gate-bulk (V_{GB}), and gate-source (V_{GS}) voltages never exceed V_{MAX}, which is define by the foundry. Only these voltages are problematic in HV designs as long as the breakdown voltage is not exceeded for drain-source voltage (V_{DS}) [10]. Biasing voltage V_{CP} and V_{CN} protect the structure by restraining the voltage nodes V_{D3} and V_{D4} to rise above V_{MAX} (3.63 V in our case) as well as V_{OUT_H} and V_{OUT_H}* to fall to low so that V_{DDH}-V_{OUT_H} >V_{MAX}. When V_{IN} is high, V_{D1}, V_{D3} and V_{OUT_H} are pulled down, whereas V_{D2}, V_{D4} and V_{OUT_H}* go up. As the M5 and M7 drains go to the ground, transistor M3 will shut-down when V_{OUT_H} reaches V_{CP} + $|V_{THP}|$. As its counterpart, M2 and M4 drains rise to V_{DDH} while M6 is cut-off when V_{D4} reaches VCN-$|V_{THN}|$. To effectively protect the overall structure, VCN must be set so that V_{CN}-$|V_{THN}|$<V_{MAX}, as well as V_{CP} <V_{DDH}-V_{MAX}-V_{THP}.

One drawback of this classic architecture in Fig. 1 is that floating nets exist: *M1 and M2 drains, as well as of M7 and M8*. In [5], additional protection transistors are added to address this issue. Pull-up and pull-down resistors have also been used, but with the disadvantage of dissipating power. Another major limitation is the switching speed at lower V_{DDH}. Indeed, because the output path is discharged through the pMOS M3, the discharge rate gets sublinear whenever V_{OUT_H}<V_{CP}+$|V_{TH3}|$. Because M1 and M2 are fighting against one another as long as V_{OUT_H}>V_{DDH}-$|V_{TH2}|$, this level-shifter switching speed is diminished when V_{DDH}-V_{CP}<$|V_{TH2}|$+$|V_{TH3}|$. This impedance fight adds up to the well known impedance fight between the pMOS and nMOS in a low-voltage level-shifter. Unfortunately, transistor dimensioning is quite a limited solution since reducing V_{TH2} and V_{TH3} to minimize

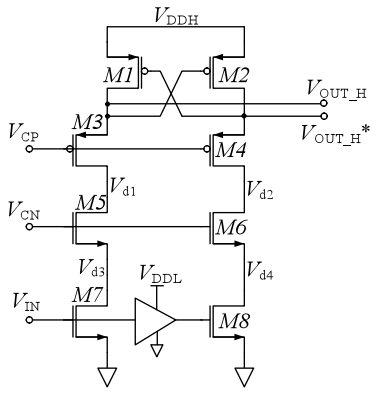

Fig. 1. Classic HV level-shifter as found in the litterature.

operating V_{DDH} will unbalance the pMOS/nMOS impedance fight preventing the level-shifter from switching. Sizing up the nMOS along with the pMOS increases the design size and also slows it down.

To boost-up the speed of the classic HV level-shifter, the authors in [6] added an inverter between M2 and M1 gates as well as AC coupling between M2 and M8 gates using a 4 pF high-voltage capacitor. The drawback of this approach is the integrated large capacitor. In a design where several HV level-shifters are required, such large capacitor is too area consuming. Other techniques have been used, but utilize DMOS, high-voltage capacitors or draw a static current.

This paper proposes a novel approach to boost the switching speed of a conventional HV level-shifter, using only near minimal size transistors, except for the high-voltage protection biasing, which can be shared, and the output buffer, while keeping a zero static power. The complete schematic, detailed in Fig. 2, is composed of four distinct structures. A HV level-shifter, which is the same as the classic one in Fig. 1, two pulse-triggered structures, added to rapidly shut-down transistors M1 and M2 when required, and an output buffer structure to drive heavier loads without sizing-up the whole structure. This output stage generates simultaneously HV protected signals for nMOS and pMOS transistors (*OUTP*, *OUTPB*, *OUTN* and *OUTNB*) and a full-scale output (*OUTF*). The output buffer uses transistors approximately 5 times of that a minimum size transistor. The bias generator supplies the whole circuit with 3 protection biasing voltages: $V_{DDH}/3$, $V_{DDH}/2$ *and* $2{\cdot}V_{DDH}/3$. The choosing of those specific values will be detailed in the subsequent section.

B. Pulse-Triggered HV LS and Protection Biasing Voltages

The HV Level-Shifter structure in Fig. 2 is no different of that in Fig. 1. However, as stated in Section II-a, this structure suffers from diminished switching speed when V_{DDH} is getting closer to V_{CP}+$|V_{TH2}|$+$|V_{TH3}|$ due to M3 and M4. The proposed HV LS presented in Fig. 2 palliates to this impedance problem. Pulse-triggered structures are added to rapidly shut-down M1 or M2 when needed. They act as active pull-ups, while requiring no static current. When M8 is turned ON (V_{IN} has fallen down) by V_{IN_IB} signal, a pulse is generated at V_{Pulse1} in the opposite branch of the LS (Pulse-Trigger #1) by the NOR gate using V_{IN} signal and a delayed inverted version, V_{IN_IB}. This pulse signal turns ON transistor M_{b5} and current flows through M_{b1}, activating M_{b2} and rapidly charging M2 gate to V_{DDH} shutting it down. V_{OUT_H}* is then easily discharged through M4, M6 and M8, which turns ON M_{b3} transistor, thus, along with the end of pulse V_{Pulse1}, turning OFF both M_{b1} and M_{b2}. This shuts down any current in the pulse-trigger branch as it resets it for the next fall on V_{IN}. Proper sizing of M_{b2}, M_{b3} and M_{b5} along with V_{pulse1} width are to be done to minimize dynamic current consumption. This pulse needs to last long enough so that M2 is shut-down rapidly but short enough to minimize the current sinked through M_{b5}. The same logic can be applied in the mirror branch (Pulse-Trigger #2).

The proposed HV PTLS was targeted at TSMC 55 nm eFlash uLP 3.3 V CMOS technology with a V_{MAX} of 3.63 V.

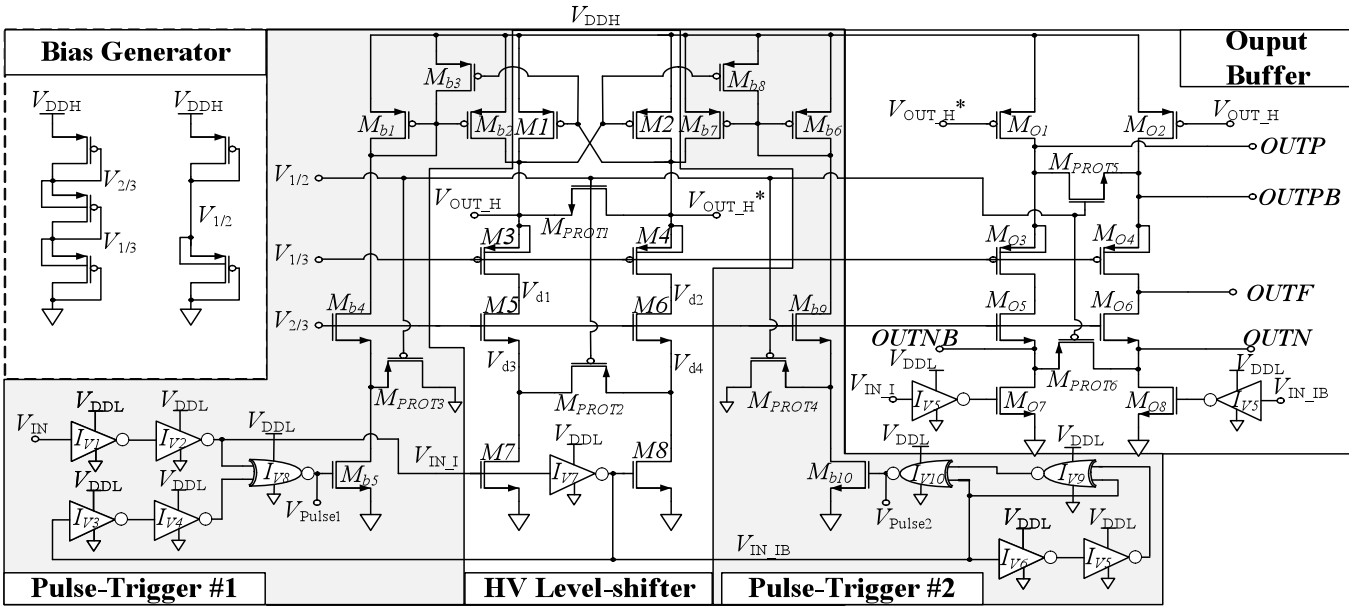

Fig. 2. Proposed fast HV level-shifter with boost technique

This PTLS can safely be used in a USB charging module operating at 5.5 V. Several topologies uses $V_{DDH}/2$ as a protection biasing voltage, as in [1] and [6]. To maximize pMOS output swing, *OUTP* needs to toggle between V_{DDH} and V_{DDH}-$V_{1/3}$-$|V_{thp}| < V_{MAX}$, where V_{DDH} is 5.5 V and V_{MAX} is 3.63 V. The minimum voltage where *OUTP* or *OUTPB* can drop is then 1.87 V. For the nMOS, *OUTN* and *OUTNB* maximum voltages are 3.63 V. Biasing protection voltages $V_{2/3}$ would then be 3.63 V ($0.66 \cdot V_{DDH}$) and $V_{1/3}$ 1.87 V ($0.34 \cdot V_{DDH}$). *OUTP*, *OUTN* and their complements are part of the floating level-shifter outputs, where *OUT_F* is the full-scale version swinging from V_{DDH} to ground.

The bias generator modules are voltage dividers of V_{DDH}. The first voltage divider generates $V_{DDH}/3$ and $2 \cdot V_{DDH}/3$ using three stacked pMOS transistors with local bulks. By using near identical size transistors, the bias voltages generated is ensured to be close to process and temperature independent, tracking V_{DDH} with precision. The second biasing branch is using the same idea but divides V_{DDH} by 2. Transistors M_{PROTn} are added as floating nets protection. pMOS type transistors with $V_{1/2}$ gate biasing ensure that their drain and source voltages will never rise above $V_{1/2} + |V_{THP}|$. If so, the excess charges are sinked into the ground through the opposite low-impedance branch of the LS. nMOS type transistors with $V_{1/2}$ gate biasing ensure that their drain and source voltages will never drop below $V_{1/2} - |V_{THN}|$. If so, this net will source charges from V_{DDH}, once again through the opposite low-impedance branch. It is to be noted that, in this proposed LS, nMOS are chosen not to have local bulks as a more convenient solution. Therefore this protection limit, affected by the body effect, is lower but still high enough to ensure pMOS transistors protection.

III. Results

The proposed HV Pulse-Triggered-Level-Shifter is targeted at TSMC 55 nm eFlash uLP 3.3 V CMOS technology with a V_{MAX} of 3.63 V for V_{GS}, V_{GD} and V_{GB} voltages. The layout occupies a surface of 26 µm × 20 µm. This level-shifter was intensely validated using SPICE simulations for every technology corners: *TT, FF, SS, SF, FS*. Moreover, for every corner, performances are ensure for a wide range of operating temperatures (from -40 °C up to 125 °C), for V_{DDH} of 2.6 V and 5.5 V, and for output capacitive loads (C_{LOAD}) up to 250 fF on every output nodes (1.25 pF). Place and route parasitic capacitances of 1 fF are also added at every schematic nodes.

A. Transient Analysis

Fig. 3 depicts the pMOS and nMOS outputs signals of the PTLS floating level-shifter, *OUTP* and *OUTN*, and as for the full-scale output, OUTF. V_{IN} is generated through a minimal size inverter, which takes as an input an ideal pulse source generator of 2.6 V of amplitude with rising and falling edges of 100 ps. Thus V_{IN} input signal follows the same corners and operating conditions described earlier in this section. Fig. 3 is a simulation for typical operating conditions: *TT, 25 °C, C_{LOAD} 100 fF, V_{DDH} 5.5 V*. The measured delays on Fig. 3, labeled as D1 and D2, refer to the rising and falling edge delays compared to that of V_{IN} for *OUTP,* at 90% of its final value. The measured values are 1.52 ns and 2.39 ns. D3 and D4 are the nMOS output rising and falling delays toward V_{IN}, also at 90% of its final value. The measured values are 1.92 ns and 1.23 ns for *OUTN* output. The rising and falling times of *OUTP* are 1.06 ns and 1.43 ns respectively and swings between 5.5 V and 2.46 V ($V_{DDH}/3 + |V_{THP}|$) which is indicated by LpMOS on Fig. 3. *OUTN* output rising and falling times are 1.02 ns and 1.38 ns respectively and swings between ground and 2.60 V ($2 \cdot V_{DDH}/3 - V_{THN} - V_{BODY}$), which is indicated by HnMOS on Fig. 3, where V_{BODY} is the body effect of nMOS transistor M_{O6}.

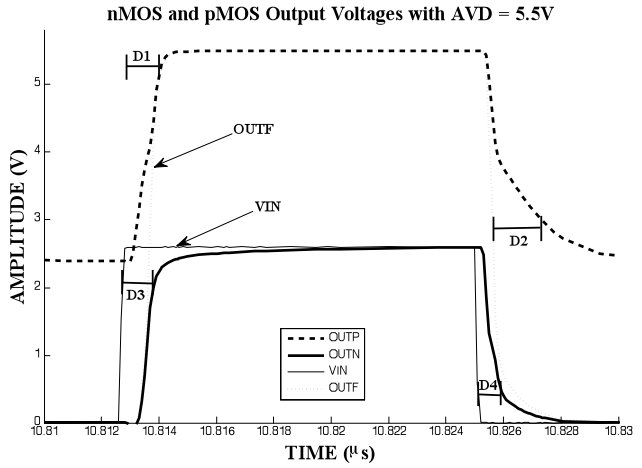

Fig. 3. Simulated ouptuts of the HV level-shifter with typical conditions for an input V_{IN} of 40MHz with V_{DDH} of 5.5V.

B. *Worst Cases Analysis*

Complete simulations for process, temperature, V_{DDH} and C_{LOAD} variations were done. The complete summary of those analysis are in TABLE I, where RT_{OUTx} and FT_{OUTx} are the rising and falling time of its respective output (x), I_{STAT} the static current consumption and I_{DYN} the dynamic average power consumption per MHz (µW/MHz). The worst case is to be found at a low V_{DDH} (2.6 V) at maximum C_{LOAD} (250 fF). The maximum rising and falling delay are respectively 10.4 ns and 5.46 ns. The cumulated simulations show that in the worst case conditions, the maximum operating frequency is 55.5 MHz when V_{DDH} is 2.6 V. However, this maximum frequency jumps up to 168.9 MHz at 5.5 V where the typical maximal operating frequency is 261.8 MHz. pMOS outputs never drop below 2.19 V and nMOS outputs never rise above 2.83 V at V_{DDH} of 5.5 V, which corroborate that this proposed HV level-shifter always respects the V_{MAX} condition.

IV. Conclusion

This paper presented a combined floating and full-scale HV level-shifter in a 55 nm 3.3 V CMOS technology. The novel approach makes the use of simple Pulse-Triggered structures to accelerate switching time, while requiring few and near minimum size transistors for the whole structure, with the exception of the output buffer and biasing, for a silicon area is 26 µm × 20 µm. We achieved a maximum operating voltage of 5.5 V while ensuring that no 3.3 V transistor exceeds the safe maximum operating voltage of 3.63 V for every V_{GD}, V_{GS}, V_{DS} and V_{GB}. Extensive simulations over process, temperature, operating voltage and output load was done to validate performances reliability of the proposed circuit. This HV PTLS shows a typical maximum delay of 2.39 ns with a worst case of 4.6 ns for respective maximum operating speeds of 261.8 MHz and 168.9 MHz at 5.5 V. This circuit shows good performances at V_{DDH} of 2.6 V, which could be pulled lower with strategic contextual gate connections of cascode and protection transistors (M_{Protn}). Moreover, C_{LOAD} and maximum operating frequency could be improved since optimization efforts were aimed on switching the speed. Finally, this HV level-shifter do not consumes any static power and shows a low µW/MHz figure.

TABLE I. Complete Worst Case Characterization of the Proposed HV Pulse-Triggered Level-Shifter

	V_{DDH}=2.6 V		C_{LOAD}=250 fF		
	Min	**Max**		**Min**	**Max**
I_{STAT} (nA)	3.1	7.0	D1 (ns)	4.6	10.4
P_{DYN} (µW/MHz)	5.7	7.7	D2 (ns)	3.3	5.5
LpMOS (V)	1.37	1.61	D3 (ns)	5.7	9.4
HnMOS (V)	0.786	1.04	D4 (ns)	1.9	2.9
RT_{OUTP} (ns)	3.4	8.0	FT_{OUTP} (ns)	2.5	4.0
FT_{OUTN} (ns)	0.293	0.677	RT_{OUTN} (ns)	3.3	5.0
	V_{DDH}=5.5 V		C_{LOAD}=250 fF		
	Min	**Max**		**Min**	**Max**
I_{STAT} (nA)	5.2	33.4	D1 (ns)	1.6	2.7
P_{DYN} (µW/MHz)	30.9	40.4	D2 (ns)	2.7	4.6
LpMOS (V)	2.39	2.63	D3 (ns)	2.1	3.9
HnMOS (V)	2.43	2.68	D4 (ns)	1.1	2.1
RT_{OUTP} (ns)	1.2	1.9	FT_{OUTP} (ns)	1.9	3.2
FT_{OUTN} (ns)	1.3	2.3	RT_{OUTN} (ns)	0.465	0.891

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