Spinner System by Dolphin Integration: optimized design and integration methodology based on pulsed latch for drastic area reduction in logic designs

Systems-on-a-chip (SoC) design complexity is continuously increasing over the years, and 100 Million gates circuits are now taping out. Additionally, the logic gate count has evolved so as to represent in average 50% of total SoC area. This rapid increase in the circuit complexity and the necessity to reduce costs, have resulted in a need for ultra high-density standard cell libraries.

For the majority of Silicon IPs providers, the area reduction of standard cell libraries, whatever is the technological process, is centered on the reduction of the number of tracks: speed critical designs rely on 12-tracks libraries, general purpose circuits leverage on 9-10-tracks libraries, while density optimized circuits are generally implemented with 6-7-tracks libraries.

Another path to improve the density of logic parts of the SoCs is to focus on the optimization of sequential cells, as 40% of logic area is generally made of sequential cells.

Like this, a new generation of standard cell libraries addresses the need for ultra high-density logic design through the use of low track cells, combined with pulsed latch cells, as the densest alternative to flip-flops.

As only less than 10% of designs are implemented with pulsed latches, it is essential to understand the principle and the art of using pulsed latch cells to reach the best density, together with the smoothest integration.

This article introduces the best technique for designing and implementing pulsed latch cells.
You will know more about the major differences between pulsed latches and flip-flops. The article also presents the spinner system as developed by Dolphin Integration including optimized pulsed latch combined with pulse generator and methodology for seamless integration within standard implementation flow, which you can rely on to achieve unexpected density results. The last part of the article will be focused on practical examples proving the benefits of the spinner system for improving the density of designs at 65 nm.

About the difference between pulsed latches and standard flip-flops

There are two main design approaches to sequential cells for synchronous memorization in logic design: flip-flop and pulsed latch.

If we have a look at their respective schematics, pulsed latches and flip-flops are fundamentally different:

1. A flip-flop is composed of 2 memorization stages (master and slave) that are basically latches (figure 1). These 2 memorization stages enable flip-flop to memorize data on a defined rising or falling clock edge, while keeping the memorized data until the next edge.
2. On the opposite, the pulsed latch memorization stage is composed of a single latch (figure 1). It memorizes data on a defined high or low state.

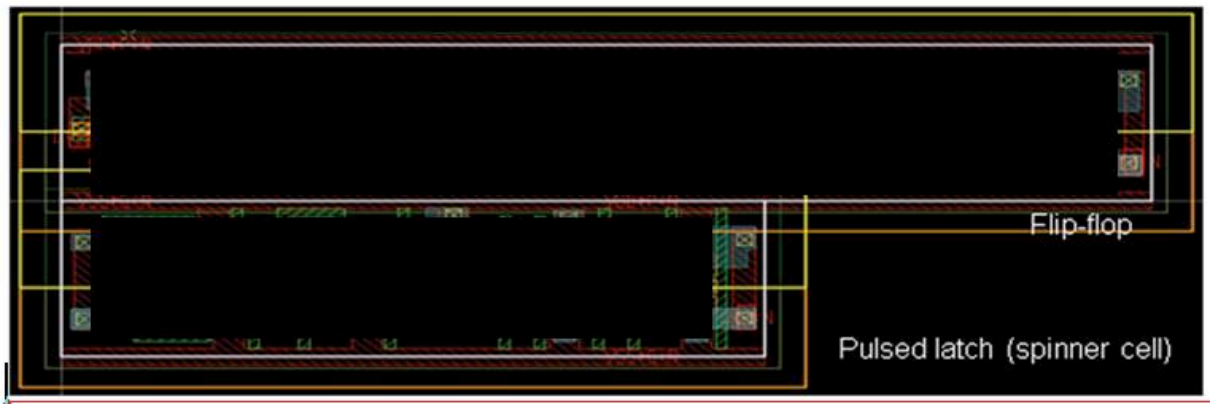

Figure 1: Flip-Flop and pulsed latch structures

The second major difference between flip-flop and pulsed latch is the clock scheme. Only flip-flop cells can be placed in standard synthesis and place and route design flows. For this reason, IP providers should model pulsed latch as a flip-flop to enable a seamless implementation in a standard design flow.
This modeling relies on the duration of the memorization state of the pulsed latch: the shortest the duration of this state is in the latch, the more it looks like an activation edge of a flip flop (figure 2). At the limit a zero state duration is an edge event.
The intent of pulsed latch cells as developed by Dolphin Integration (spinner system), is to transform clock signal to a pulse at the clock input of the latch to emulate a flip-flop behavior.

Figure 2: Clock scheme difference between flip-flop and pulsed latch

If we perform a comparison at cell level, the replacement of flip-flop by pulsed latch has undeniable benefits (table 1).

65 nm	Area (um²)
Dolphin's 6-Track Flip-Flop	8.64
Dolphin's 6-Track Pulsed latch as spinner system	6

Table 1: Comparative cell density of pulsed-latch and flip-flop

Taking as an example Dolphin Integration's 65 nm standard cell libraries, the replacement of conventional flip-flop by pulsed latch as "spinner system" leads to 30% of area savings at the cell level.

Pulsed latch cells as developed by Dolphin Integration

Designing with pulsed latches is not a widespread practice as pulsed latch cells available on the market present some significant drawbacks. Only custom designs used pulsed latch circuitry to improve density but also power consumption.

Firstly, as designers need to optimize the pulsed clock, clock path synthesis and static timing analysis are far more tortuous. The other downside of pulsed latch is the increased number of hold time violations compared to flip flop designs, so much that logic with pulsed latches finally tends to have the same density after routing than with flip-flops.

The mandatory adaptation of the pulsed latch circuitry to the use by APR in automated physical implementation of logic design has resulted in the development of the "spinner cell" system by Dolphin Integration.

The key challenge of this adaptation is the automated and safe design of a clock network propagating a pulse to the clock input of the spinner cell. For sake of simplicity and smooth usage, Dolphin Integration has developed a unique methodology relying on APR clock-tree generation with automated changes enabling a seamless integration in the traditional Users' physical implementation flow.

This methodology is based on the introduction of additional but automated step at clock tree generation and related check at signoff step (figure 3). The pulse generator insertion is patented (1).

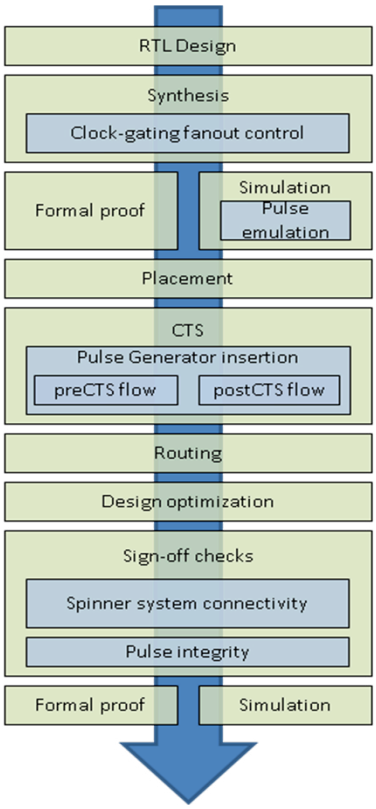

Figure 3: Physical implementation design flow for spinner cell based implementation.
Blue boxes indicate steps for which spinner cell dedicated settings or actions are provided.

Dolphin Integration's methodology relies on the "Insert pulse generation" script ensuring automated substitution of some clock-tree buffers by pulse generator after clock tree generation in APR (figure 4). For the designer, implementing with spinner system is as simple as implementing with flip-flops. The script is compatible with most of the physical implementation flows and sign-off checks available on the market.

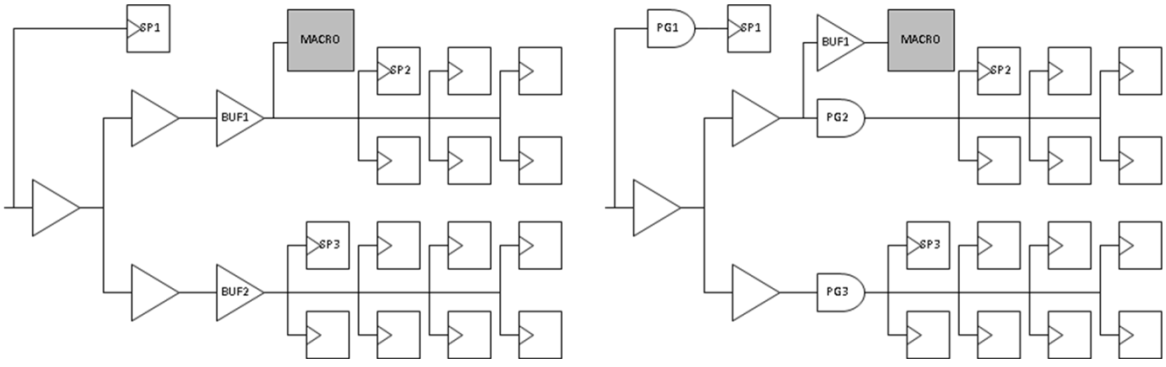

Figure 4: Spinner clock tree prior and after substitution
Triangle stands for clock buffers, rounded rectangle with PG for pulse generator and rectangle for pulse latches (clear) and macros (grey)

To avoid the usual tricks of timing closure for design based on latches, spinner cells are described as flip-flop at liberty level. This description relies on no-change timing

convention instead of conventional setup-hold at liberty level. As this is completely supported by common APR flows and signoff timing tools, it does not introduce any change in design flow.

The minimization of hold time violations has the objective to maintain the same placement density as with flip-flops.

The use of pulse at the clock input of the spinner cells described as flip-flops implies that pulse duration is added to the hold constraint of the cell in hold time timing checks. The hold time correction may induce area increase after clock tree step in logic design.

An innovative and patented[2] feature has been developed to reduce the hold time correction at spinner cell level without impacting required pulse width. It enable to design the spinner cell to have the lowest possible minimum pulse width on clock input with the highest possible hold time corrected inside the cell as illustrated (figure 5) below for a spinner cell with scan feature.

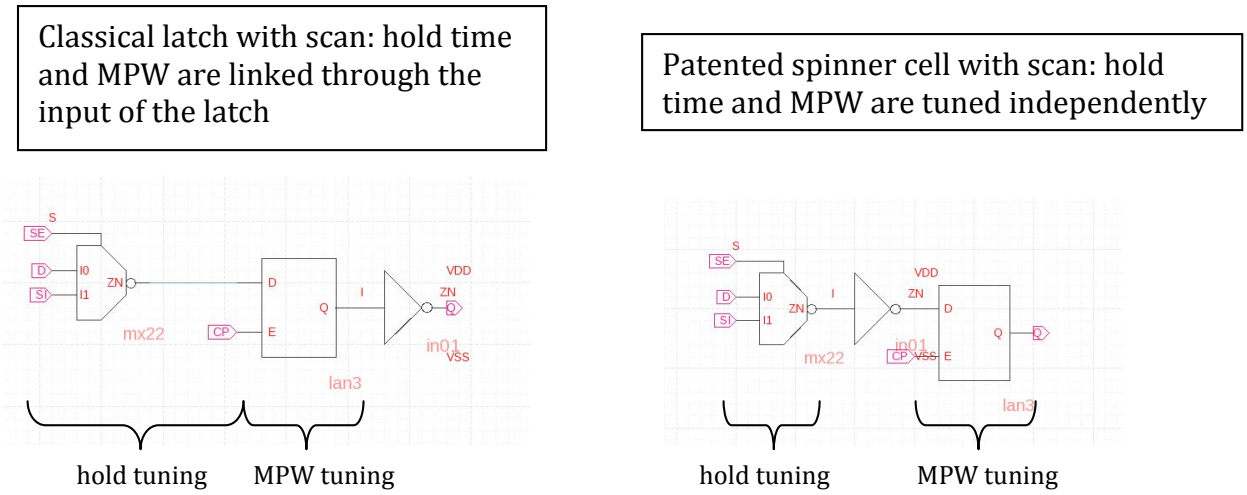

Figure 5: Independent hold time and Min Pulse Width (MPW) tuning in patented spinner cells

Also, as a pulsed latch is generally more sensitive to process variations, the robustness of the spinner system has been assessed in an exhaustive combination of process, voltage, power supply and usage conditions including mismatch simulation to ensure a right-on-first-pass design. Pulse variability is taken into account at design level through fixed and variable On Chip Variation (OCV) margins.

Drastic area reduction of logic design with pulsed latch cells as "spinner system"

The example below based on post Placement and Routing benchmark results on real conditions proves the benefits of the spinner system for improving the density of designs at 65 nm LP process.

The comparison has been done between 2 standard cell libraries:

- Dolphin Integration's SESAME HD, 6-Track standard cell library with classical D-flip flops
- Dolphin Integration's SESAME uHD-BTF, which is the same 6-Track standard cell library where only D flip-flops have been replaced by spinner system (all combinatorial cells are identical)

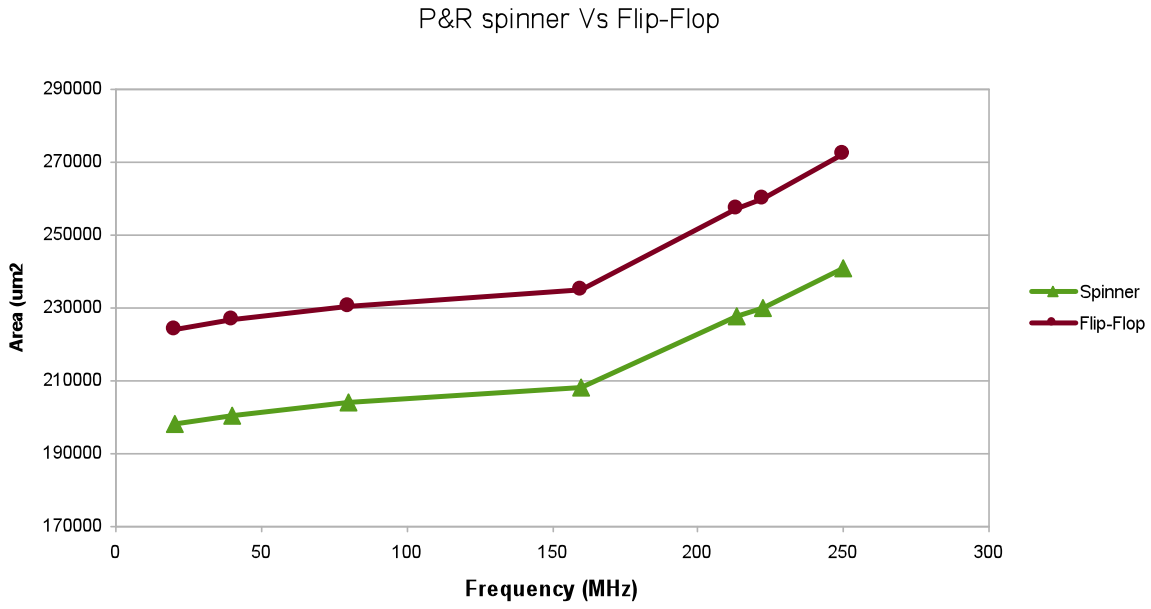

Figure 6: Spinner system performances on real circuit at 65 nm

Highlights:

- SESAME uHD-BTF standard cell is roughly **10% denser** after P&R compared to SESAME HD standard cell

Summary

This paper introduces the Spinner System. Based on the pulsed latch principle, the Spinner System proposes a couple of two cells (spinner cell + pulse generator) and a smooth implementation flow to achieve significant area reduction. Post placement and routing results in TSMC 65 nm shows 10% area reduction and illustrate how pulsed latch through the Spinner System can help designers to address the needs for ultra high-density logic design.
The spinner system as developed by Dolphin Integration has proven its benefits towards smaller logic design not only in mature technological processes such as 180 nm, 130 nm but also in most advanced processes such as 65/55 nm, and 40 nm.

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[1] FR2963688 (A1) - 2012-02-10 - ARBRE D'HORLOGE POUR BASCULES COMMANDEES PAR IMPULSIONS

US2012032721 (A1) - 2012-02-09 - CLOCK TREE FOR PULSED LATCHES

[2] FR2972087 (A1) - 2012-08-31 - Circuit de bascule commandée par impulsions

About the author

Lionel Juré
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Lionel Juré joined Dolphin Integration in 2001 and is the lead design engineer for standard cell library product line at Dolphin Integration.
Lionel was previously development manager for the memory product line at Dolphin Integration. He started his professional life in layout of analog silicon IPs for 2 years.

Lionel earned is PHD in physics from the University of Grenoble, France.

About Dolphin Integration

Dolphin Integration contribute to "enabling mixed signal Systems-on-Chip". Their focus is to supply worldwide customers with fault-free, high-yield and reliable kits of CMOS Virtual Components of Silicon IP, based on innovative libraries of standard cells, flexible registers and low-power memories. They provide high-resolution converters for audio and measurement, regulators for efficient power supply networks, application optimized micro-controllers.
They put emphasis on resilience to noise and drastic reductions of power-consumption at system level, thanks to their own EDA solutions missing on the market for Application Hardware Modeling as well as early Power and Noise assessment. Such diverse experience in ASIC/SoC design and fabrication, plus privileged foundry portal even for small or medium volumes, makes them a genuine one-stop shop covering all customers' needs for specific requests. http://www.dolphin-integration.com