SLED 3.3 & SMASH 7.3

Make schematics meaningful with colors

SLED 3.3 enables background coloring and patterning of each individual symbol instance. This feature aims to make schematic more meaningful by enabling easy customization of symbol instances of a same cell.

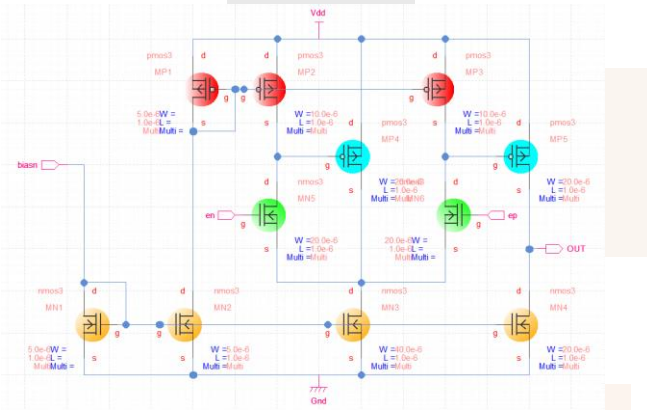

Fig 1: Colorization of individual instance

Improved parameters

- SLED 3.3 finalizes parameter migration for multi-level schematics. From now on, parameter definition is only allowed on cells.
- In addition to this migration, SLED 3.3 also enables adding unit and description attributes to parameters. These new attributes make parameter easier to understand for more intuitive use.
- Associated with the migration, the interface for editing parameters has been improved:
    - A new search field makes it easy to find a parameter.
    - A new filter button that displays only relevant parameters related to current design context

Improve quality control of your schematics

SLED 3.3 provides new API functions for defining and adding new DRC rules to the SLED DRC engine.
These new DRC rules must be implemented in a TCL script and can be used to add checks on symbols, schematics, and cells.
These new rules can be configured and used just as the SLED's built-in DRC rules (assertion level setting, execution, and visualization of results).

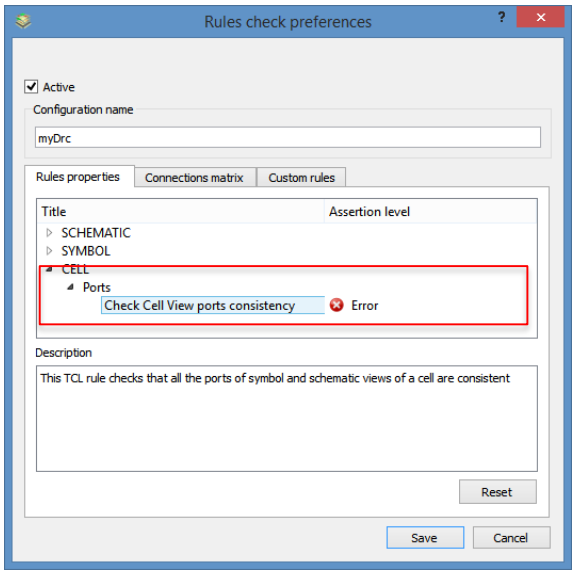

Fig 2: Rules check preferences

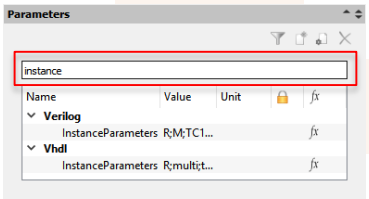

Fig 3: Usage of the parameter search field

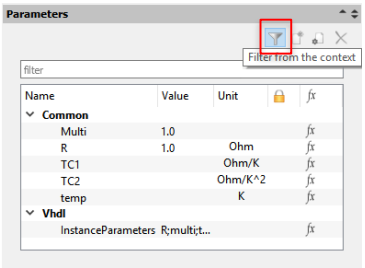

Fig 4: Parameter filtering by context

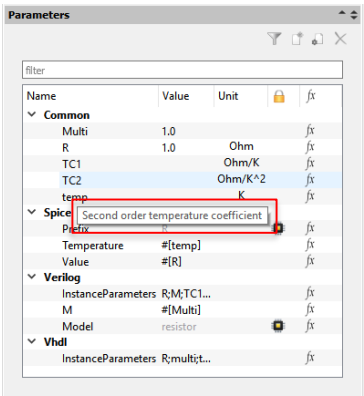

Fig 5: Unit and description of the parameter

SLED 3.3 & SMASH 7.3

FIND EXHAUSTIVE LIST OF OPERATING-POINTS

With this new CMOSLogic method used for multiple operating-points analysis, SMASH 7.3 provides designers with a solution for obtaining an exhaustive list of all possible combinations of stable operating-points of a CMOS logic circuit. This feature simplifies and speeds up the characterization of multi-bit standard cells.

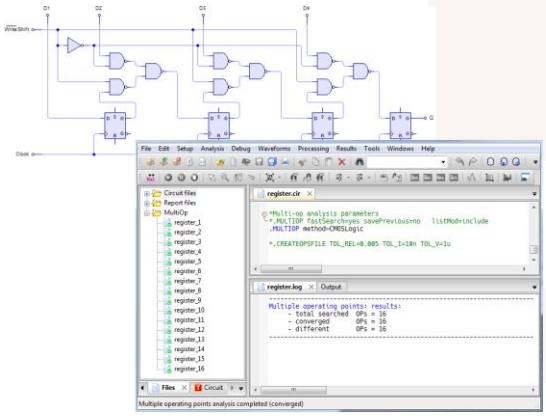

Fig 6: Exhaustive list of all possible operating points

SPICE MODEL UPDATE

BSIM-IMG 102.9.1 model is the last release of BSIM Independent Multi-Gate Model from the BSIM Group. BSIM-IMG is an industry standard for FDSOI transistor simulations.

UTSOI v2.20 model is the last release of UTSOI model developed by technology research institute CEA-Leti. The Leti-UTSOI compact model was developed to describe the electrical behavior of FDSOI transistor taking into account all its specificities. In its latest version (2.0), the Leti-UTSOI compact model includes the full description of the creation of an inversion layer at the rear face of the silicon film.

RESISTOR R3_CMC model is a nonlinear 3-terminal resistor model that includes self-heating, velocity saturation, statistical variations, and parasitic capacitance and currents.

TMI2 SUPPORT

SMASH 7.3 supports the last TSMC Model Interface (TMI2). The TSMC Modeling Interface is a C based modeling API developed to enable more accurate layout-dependent effect which are modeling on top of standard SPICE models.
TMI2 also provides an unified infrastructure to address the emerging nanometer effects associated with 40nm technology and beyond like: statistical models, aging models, self-heating models and restricted design rules.

S-PARAMETERS EXTRACTION

SMASH 7.3 provides the possibility to extract S-parameter and to generate Touchstone file from any circuit in small signal analysis, thanks to the .LIN directive and the port P element device.
The S-Parameter device models the n-port network device defined in a Touchstone file that contains the parameter data of active or passive devices, or interconnect networks.

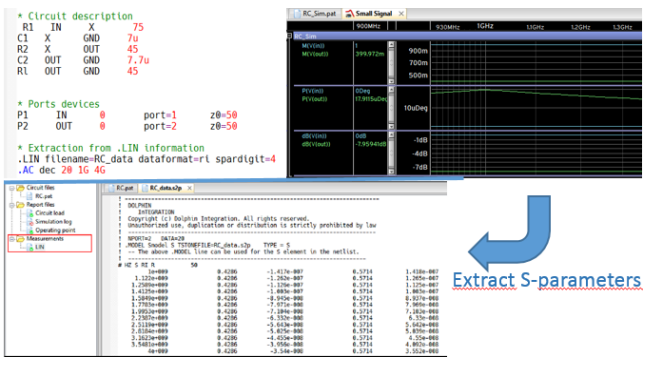

Fig 7: Extraction of S-parameters

YOUR FEEDBACK MATTERS

To contribute suggestions and requests for the Dolphin EDA Solutions, please provide feedback on your user experience to **support@dolphin.fr**