The Enabler of Low-Power Systems-on-Chip

DOLPHIN INTEGRATION

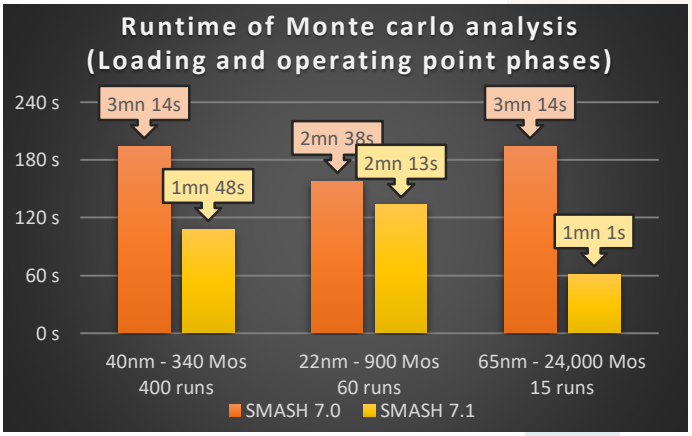
SLED 3.1 & SMASH 7.1

EDA Solutions
Missing EDA Links

OPTIMIZE MONTE CARLO ANALYSIS

Accelerating Monte Carlo Analysis is crucial because designs in advanced process-node have much larger variation and need to run thousands or even millions of statistical simulations.

Thus, with SMASH 7.1, for circuits with thousands of MOS devices, Monte Carlo analysis has been sped-up by accelerating loading phase of each run by a factor of up to x3.



NETLISTER SPEED IMPROVEMENT

In SLED 3.1, speed of netlister has been improved by a factor of x2, especially on large designs.

SIMULATE S-PARAMETER DEVICES

SMASH 7.1 introduces S-Parameter devices.

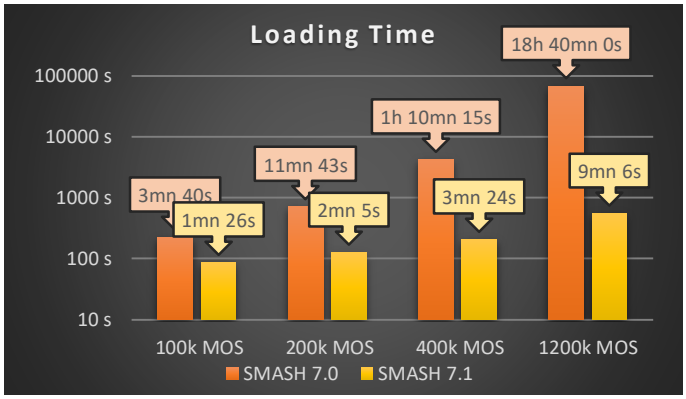
S-Parameters describe the behavior of linear electrical n-port networks.
SMASH supports S-Parameter devices defined by Touchstone file format (version 1.0 or 2.0). Touchstone files contain information about parameter data of linear active devices, passive filters, passive devices, or interconnect networks.

SMASH 7.1 supports S-Parameters devices for operating-point analysis, small signal (AC) and large signal (DC) analyses.

ANALOG DESIGN WITH MILLIONS OF MOS

Since releases 7.0, as a 64-bit native application, SMASH handles larger circuits such as memories with millions of MOS transistors.

With SMASH 7.1, the loading time and the memory consumption of these large circuits have been substantially improved. The loading time is improved by a factor of up to x100, and the memory consumption is reduced by 30%.



FFT AND JITTER

SMASH 7.1 improves handling of .FFT and .JITTER directives to enable their use in sub-circuit instances and to automatically generate the required waveforms (with implicit .PRINT directives).

test_1.pat

```
SP0 IN OUT0 mname=model_s0

.model model_s0 S TSTONEFILE = touchstone_file.s2p
+ INTERPOLATION = LINEAR
+ LOWPASS       = 2
+ HIGHPASS      = 0
```

touchstone_file.s2p

```
# MHZ S MA R 10000
 8.7500000  0.00357593049000 -174.62200000000  0.993
17.5000000  0.00362742894000 -169.35100000000  0.993
26.2500000  0.00371173455000 -164.28300000000  0.993
35.0000000  0.00382659957000 -159.49300000000  0.993
43.7500000  0.00396946656000 -155.03200000000  0.993
52.5000000  0.00413736849000 -150.92600000000  0.993
```

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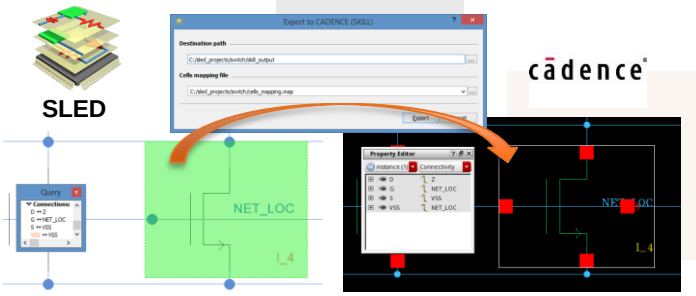
EXPORT SCHEMATICS TO CADENCE

To improve the interoperability of the Dolphin Solutions, SLED 3.1 provides a command to convert a SLED design (Libraries, Cells, Schematics, Symbols) into a CADENCE Virtuoso design.



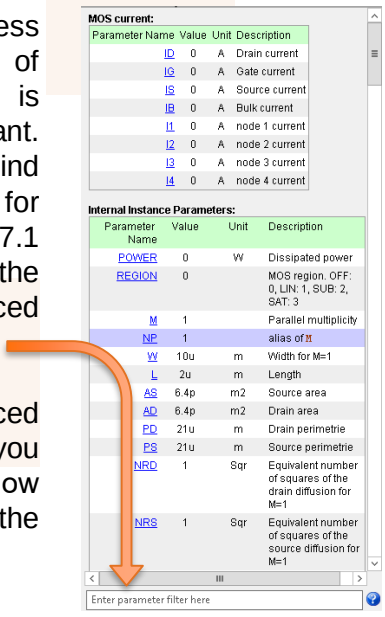
This command takes as input a mapping file that can be created using 2 scripts:

- One Tcl script to extract cells data from the SLED libraries of a design and generate a skeleton of the mapping file.
- One Skill script to extract cells data from the libraries of a CADENCE Design Kit that can then be used to complete the mapping file manually.

WAVEFORM VIEWER ENHANCEMENT

In advanced process nodes, the number of device parameters is becoming more important. To help our users find specific parameter for drawing, SMASH 7.1 provides a filter box at the bottom of the Advanced Parameters panel.

To open this Advanced Parameters panel, you have to click on the “Show Parameters” button at the top of the circuit tab.



SLED HOOKS

To allow users to adapt the behavior of SLED to their needs, SLED 3.1 provides functions to handle hooks.
User-defined C or Tcl functions associated to a hook will be executed when predefined event corresponding to the hook occur:

- sled_on_post_init
- sled_on_pre_load
- sled_on_post_save
- sled_on_pre_netlist
- … and many more

LOAD ARCHIVE

SMASH can generate circuit archives, either with the .ARCHIVE directive, or with the "Tools > Generate Archive File" menu.

To ease circuit re-use, or circuit dispatching on computer farms, archives(*) can now be loaded directly in batch mode by specifying the name of the zip file on the command line.

(*) currently available if the archived circuit contains only Spice elements

BSIM MODEL UPDATES

SMASH 7.1 includes new MOSFET model releases:

- BSIM SOI v4.5: model for SOI (Silicon-On-Insulator) circuit designs, developed by University of California, Berkeley
- BSIM-IMG 102.8: Independent Multi-Gate model, developed by University of California, Berkeley. BSIM-IMG is an industry standard for FDSOI transistor simulations.

YOUR FEEDBACK MATTERS

To contribute suggestions and requests for the Dolphin EDA Solutions, please provide feedback on your user experience to **support@dolphin-integration.com.**

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