High Speed SMASH Simulations

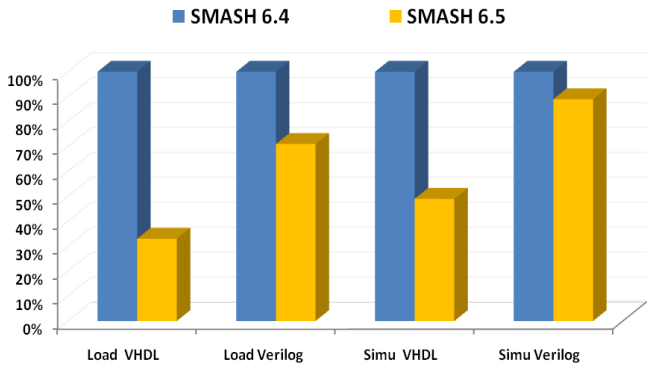
Staying on the cutting edge of simulator performance, SMASH 6.5 makes three major steps forward:

Logic simulations

- Thanks to a new optimization in the logic event-driven simulator, SMASH speeds-up simulations x2 for VHDL circuits and gains 10 % for Verilog-HDL designs.
- Loading of logic circuits is faster thanks to smart optimizations.

Analog simulations

- Analog operating-point runtime is shorter for large circuits: from x2 to x5 faster



Load and simulation runtimes for logic circuits: SMASH 6.4 vs 6.5

Other Key Features of SMASH 6.5

Analog solver: Push the limits!

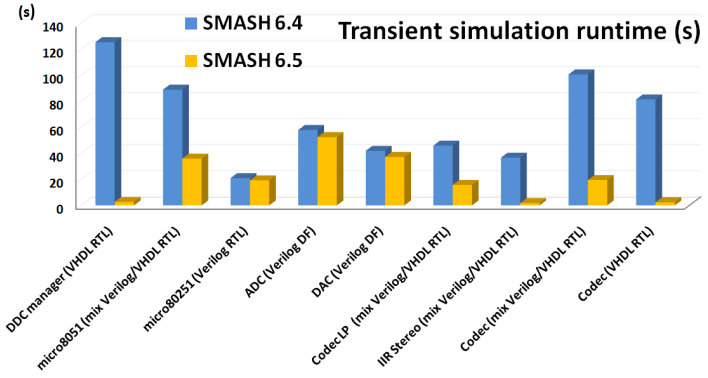
- New Analog solver is applied by default
- Merge-MOS options: speed-up (x2) simulation runtime
- Analog operating-point runtime improvement
- Model updates: UTSOI, BSIM-CMG, BSIM 6.1
- Converter of noise simulation results to Verilog-A/VHDL-AMS models

New IDE ergonomic enhancements

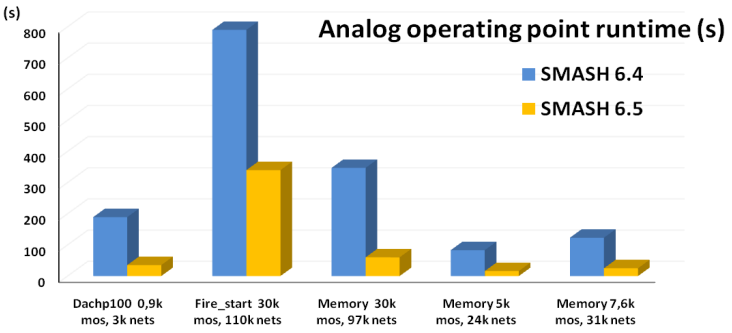
- Higher stability of the graphic user interface for enhanced ease of use.
- Improved use of Wave viewer and IDE shortcuts through remote access
- Ergonomic adjustments (drag and drop, zoom...)

New Language Support

- Verilog-A support: 'last-crossing' analog operator, port branch access



SMASH simulation runtimes for different logic circuits



Analog operating point runtimes: SMASH 6.4 vs 6.5

Focus on HDL-AMS Noise Model Converter

SMASH provides a new .CREATENOISEMODEL directive, configurable through a dialog, as a quick way to generate a noise source model that fits noise analysis simulation results. Once the model is generated, it can be used to replace the SPICE block to speed-up the simulation.

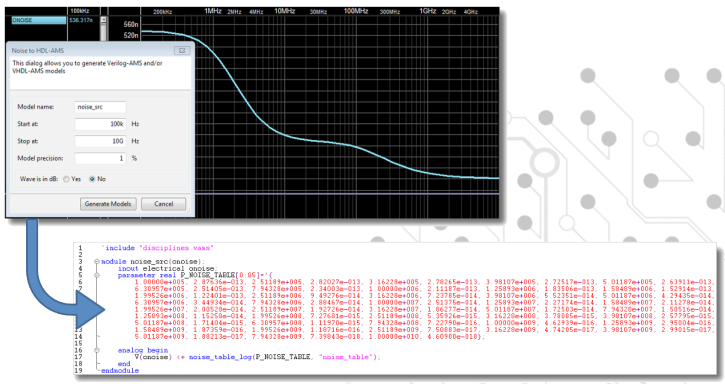


Illustration of the noise model converter dialog box and the noise HDL-AMS source model

YOUR FEEDBACK MATTERS

SMASH is known as one of the best high speed mixed-signal simulators. To contribute suggestions and requests, please provide feedback on your user experience to **contact@dolphin-ip.com.**