SMASH 6.4

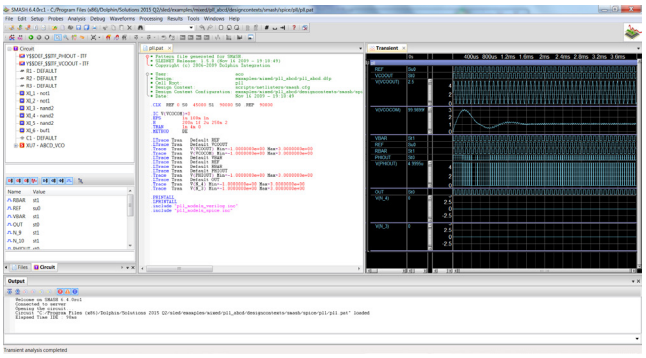
EDA Solutions

Speed-up to improve productivity

Staying on the cutting edge of simulator performance, SMASH 6.4 makes 3 major steps forward:

- Thanks to a new analog solver, SMASH shortens simulations of big analog circuits from weeks to days.
- Loading of logic circuits is up to 2 times faster thanks to the use of a new compiler.
- Better speed and memory performance under Linux with a SMASH native application.

SMASH 6.4 also delivers long-awaited features such as the "Magnetize" and "Transient Continue" and some user friendly IDE enhancements to constantly improve the overall user experience and productivity.

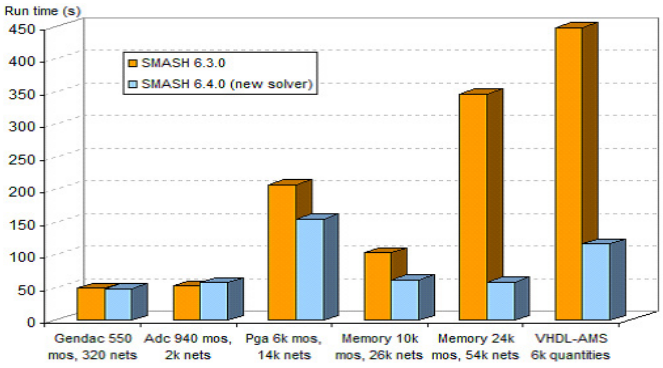


SMASH 6.4 IDE

BREAKTHROUGH

A major step forward has been realized with the implementation in SMASH of a **new analog solver.** It speeds up significantly large circuit simulations:

2x to 100x faster.



SMASH simulation run times for different circuits

Key Features of SMASH 6.4

Faster and Safer

- SMASH enables to continue transient simulations.
- With the removal of the Classic IDE and Wine, SMASH is now a native Linux application! SMASH under Linux is faster and less memory consuming, and batch tests are easier.
- Speed up loading of VHDL(-AMS) and Verilog(-AMS) netlists up to 60 % with an option to optimize compilation of HDL modules.
- Non-regression test (.NRT directive) has been extended to logic signals to compare two logic waveforms.

New IDE Ergonomics and Waveform Viewer enhancements

- Magnetize feature for interactive and deeper analysis of the analog waveforms.
- Show Reference feature for graphic comparison of analog waveforms from the same or another circuit or simulator.
- New Probe File capabilities: it is now possible to export a waveform window into the probe file with an 'add only' mode and define the scale of a waveform window.
- Better way to open included file in the text editor

YOUR FEED-BACK MATTERS

SMASH is renowned in the analog design community as a state-of-the-art mixed-signal simulator with multi language and multi level simulation capabilities. To continue enhancing the user experience, please provide feedback on your needs to **solutions@dolphin-integration.com.**

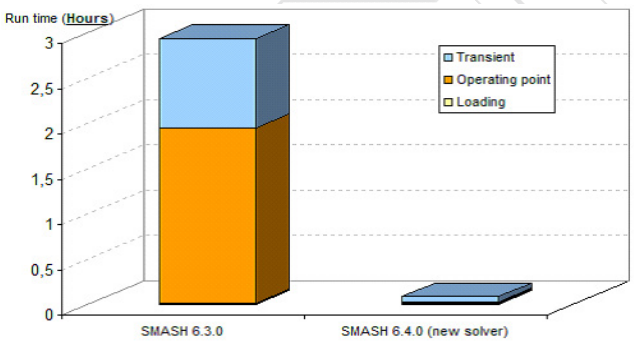
Focus on the new SMASH analog solver

Simulation run time is very crucial for any designer: it is the main obstacle to productivity and determines the achievable final verifications. On the other hand, speed without accuracy is meaningless for analog designers, this is why the new analog solver for SMASH ensures the accuracy offered by a global-convergence solver with the following advantages:

- High speed-up for large circuits,
- Increase of capacity to simulate large circuits.

Key Gains:

- SPICE memory 10kmos 25knets : **x2**
- SPICE memory 24kmos 54knets: **x7**
- VHDL-AMS 6k quantities: **x4**
- SPICE 131kmos 425knets: **x30**(transient) **x100**(operating point)



Memory 131k Mos / 425k nets : Simulation time details

Highlight on the major enhancements of the waveform viewer

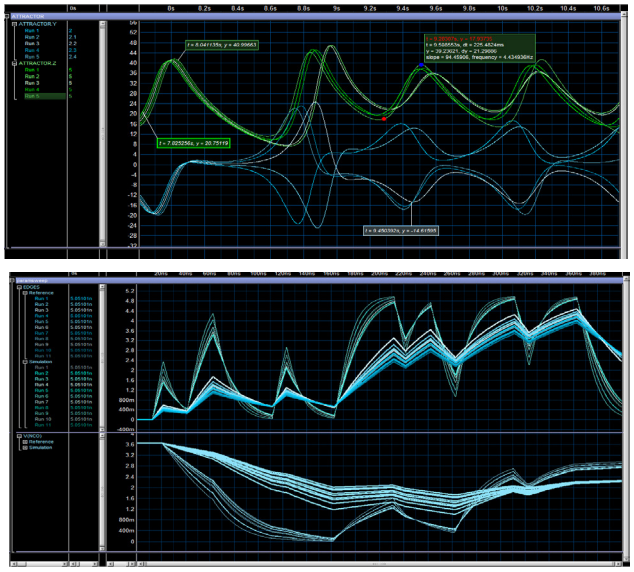
Magnetize

Magnetize is a new command which allows obtaining exact values, driven by simulation results instead of graphic approximations. The exact values of the waveforms are displayed and differences, such as propagation or rise/fall times, can be easily measured.

To support this feature, smart options are available, such as "Define Measurement Origin" to fix origin at the current point and to measure differences, or "Add Marker" to display the exact coordinates of the selected point.

Show Reference

The Show Reference command toggles the display of the reference trace of the selected graphs or waveforms. Prior to displaying a reference trace, any reference files from a previous analysis or from another circuit can be associated with a waveform view.



Magnetize (top) and Show Reference (bottom) illustrations

Focus on Logic Non Regression Test

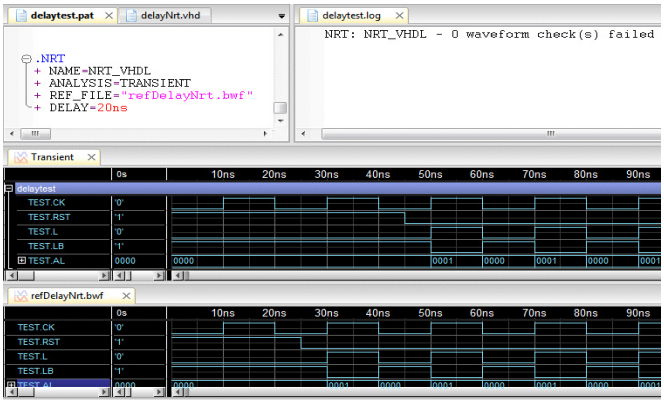


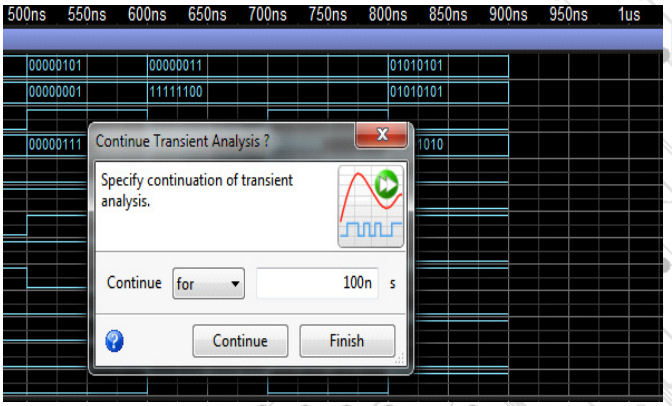
Illustration of .NRT Logic

The Logic Non-Regression Test (.NRT directive) enables checking the differences between two logic or digital waveform files (reference file vs. current simulation). This Non-Regression Test process is launched at the end of the transient analysis. It consists in verifying that each value change of a "checked" waveform matches with the corresponding "Reference" waveforms.

Different options are available for selecting the right waveform or part of this waveform: "Select list", "Window", "Sample", "Enable". Moreover, specific options enables dynamic and smart comparisons: for instance, "DY" specifies the absolute or relative y-axis tolerance and "Trunc" for a comparison of the specified vectors which ignores the Least Significant Bit.

Focus on Transient Continue

The "Allow to continue simulation" option of the Transient parameters dialog enables activating the possibility to continue the simulation when the specified End time is reached. When enabled, the dialog "Continue Transient Analysis" is opened at the end of transient analysis for allowing to continue the simulation until a new end time or forever (until the user or the testbench stops the analysis).



Continue Transient Analysis window

New Language Support

- **PWL SPICE** source instantiation from Verilog-AMS module
- Verilog-AMS **above() function**