



### SMASH NEW GENERATION

Most of our users are aware that Dolphin Integration has been preparing major changes in SMASH to increase our users' productivity with:

- → A new IDE sporting a new waveform viewer
- An upgraded implementation of the already bestin-class VHDL and VHDL-AMS language compliance and simulation engine

SMASH 6.3 cumulates these enhancements to significantly improve user experience.

### KEY FEATURES OF SMASH 6.3

- New IDE with enhanced user interface and waveform viewer
- Upgraded VHDL and VHDL-AMS implementation
  - Substantial extension of language compliance
  - Improved loading and simulation time on some designs
  - Finer debug when using breakpoints and step-by-step execution
- Integrated standard UTSOI compact model for predictive analysis of the FDSOI process
- Extended support of transient noise analysis to all noise sources
- Automatic detection of analysis runs in batch mode
- Enhanced HSPICE compatibility

Support of Safe Operating Area (SOA) checks specified in foundry model parameter sets

#### HIGHLIGHT ON THE MAJOR ENHANCEMENTS OF THE USER INTERFACE AND THE WAVEFORM VIEWER

- Smooth navigation between simulator control file, netlist / design files, and waveforms... using tabs
- Smarter management of panels
- Capability to resize, move, add or delete columns
- Creation of a hierarchy of waveform groups
- Capability to expand busses and multiple runs of Monte Carlo and Sweep analyses
- Statistics pane to display statistics of analog signals at a glance
- Use of several vertical cursors to perform measurements



Overview of SMASH mixed signal simulator



Transient noise analysis on HDL-AMS description



Overview of SMASH IDE and waveform viewer

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# SMASH 6.3



# VHDL AND VHDL-AMS NEW TECHNOLOGY

Our renowned state-of-art VHDL-AMS simulation engine has undergone a significant upgrade to provide:

- Enhanced language compliance,
- Improved loading and simulation time,
- Increased behavioral modeling and simulation capabilities with Transient Noise Analysis (TNA).

It paves the way to further speed improvements as well as to the support of VHDL 2008 and SystemVerilog.

```
2
       library ieee
       use ieee.electrical_systems.all;
use ieee.math_real.all;
 3
 5
       entity e is
       generic (f: real := 1.0e3);
end entity;
10
     \Thetaarchitecture a of e is
           quantity q1, q2: voltage;
11
12
     Obegin
13
            procedural is
14
15
                 variable var: real;
16
17
            hegin
                 var := sin(math_2_pi * f * now);
                q1 := var;
q2 := cos(3.0 * var);
18
            end procedural
20
21
      end architecture:
22
23
```

Example of procedural statement

### • Enhancements

- Large improvement of the support of aliases
- Extended support of record types for ports and generics
- Local Truncation Error (LTE) algorithm applied to VHDL-AMS simulations
- → Improved coverage reports
- More detailed debugger breakpoints and step-bystep execution
- Support of large arrays (memories), record signals and complex expressions which previously slowed down or blocked circuit loading
- Exit and next statements with loop labels to apply to the designated loop
- Improved mixity between VHDL-AMS and Verilog-A or Spice descriptions
- → Up to 2 times faster when running transient analysis

## - Your feedback matters

SMASH is renowned among the VHDL-AMS community as the simulator with the most advanced language compliance. SMASH 6.3 pushes the edge further and extend its VHDL-AMS support.

Please provide feedback on your user experience with your test cases to solutions@dolphin-integration.com.

- New features
  - Expressions as input port actuals in component instantiations
  - Subprogram declarations and definitions in more contexts (entities, architectures, processes)
  - Type declarations in more contexts (entities, processes, generate blocks)
  - → Full support of use clauses
  - References to definitions in other packages with the full name to the definition, with no use clause
  - Reference to VHDL signals in Verilog with hierarchical names
  - → VHDL-AMS
    - Simultaneous procedural statements

 Break statements on a single elements of composite quantities

- Attributes on composite, indexed or selected quantities
- Support of small signal noise analysis



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