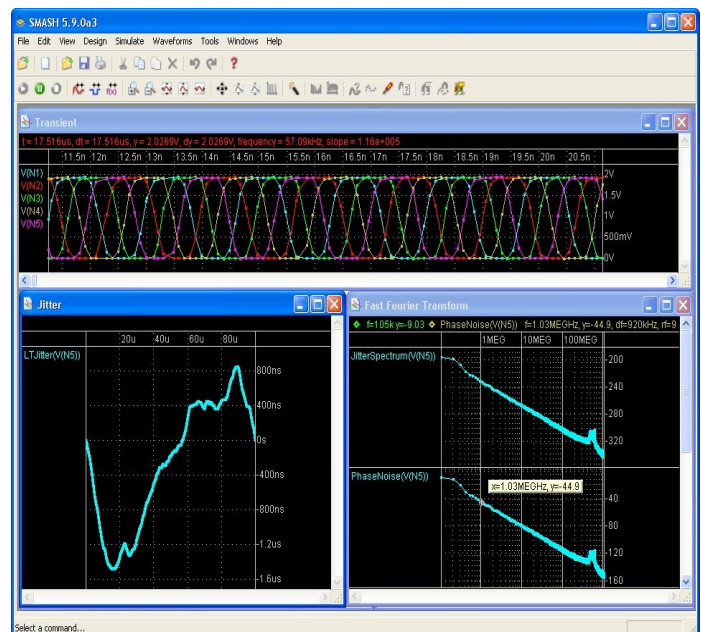


SoC developers spend 70 % of their time debugging their design and analyzing unexpected or out-of-specification results. Improving productivity is therefore essential for the time-to-market requirements of today's SoC. To that end, SMASH 5.9 introduces debug techniques, which have been successfully used in application software development, and adapts them to the world of transient simulation on HDL-AMS descriptions for efficient back-tracing on break points, in association with graphical access to the hierarchy of the design. Analog designers will appraise further improvements in their domain, such as new and updated SPICE models, phase noise extraction...

KEY ENHANCEMENTS

- ✓ Productivity-oriented enhancements of Graphic User Interface including hierarchical inspection of designs
- ✓ Interactive HDL-AMS debugging with break points, step by step and event back trace
- ✓ Phase-noise extraction on long term Jitter
- ✓ Power consumption reporting by SCROOGE to determine the impact of clock trees and optimize the selection of standard cells for synthesis
- ✓ Inductance model with magnetic core for DC-DC converters
- ✓ HSPICE compatibility improvements for full compliance with foundry model parameter files
- ✓ COSMOS cosimulation of analog and mixed-signal blocks with Simulink



DESCRIPTION OF THE ENHANCEMENTS

Graphic User Interface improvements provide the designer with a hierarchical view of the design allowing easy access to circuit elements for debugging and watching signals and variables, probing and tracing device values and parameters...

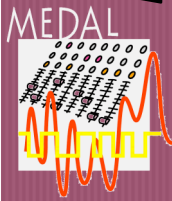
Interconnect-based high impedance net handling better detects totally high-impedance nets and takes into account internal parasitic devices such as found in the BSIM4 model to more accurately report potential errors to the designer.

Compatibility with HSPICE and foundry delivered model parameter sets has been enhanced to directly support random function syntax (AGAUSS, AUNIF...).

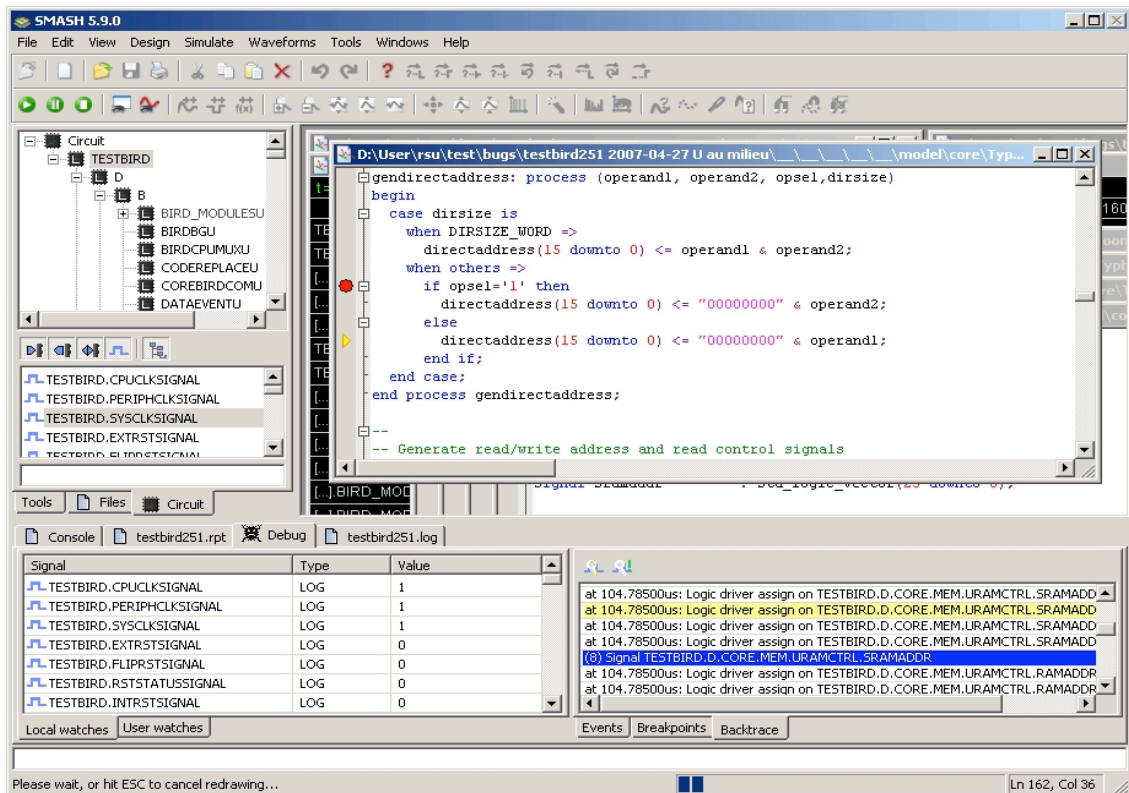
To enable efficient usage of power consumption analysis, SCROOGE hierarchically separates the emulated clock-trees from the rest of the design and generates a detailed report, including power consumption of standard cells and selected instances in the hierarchy. This enables the designer to effectively investigate the power consumption of different elements of the design and tune the synthesis to optimize selection of standard cells and reduce overall power usage.



SMASH is available identically under Linux, Solaris and Windows.



MEDAL Presentation Sheet



A **hierarchical view** of the design provides fast and direct access to the source code; by simply double-clicking on an instance, the corresponding source code will be displayed in a new editor window.

Placing **time, signal** or **source code breakpoints** makes it easier to isolate design bugs and enables **step by step** simulation. The simulation pauses when a breakpoint is reached and the designer can elect to step over **time points, delta cycles, events** or **instructions**.

Simulation can be run in **slow motion** or **animated mode** (per instruction or per simulation cycle) to help identify the cause of a design bug. A **marker** in the source code shows what will be executed next during **slow motion** simulation.

Variables, signals and quantities can be watched during the simulation for online investigation of "data" and "calculation" design bugs. **Local** watches are automatically displayed for the instance under investigation and the designer can configure **User** watches as needed.

The **simulation history, or backtrace**, keeps track of what has been previously simulated to reduce tedious step by step simulation. It provides online investigation of design "behavior" and "control" bugs by allowing to determine the data change paths in the simulation.

The **upcoming events viewer** helps to understand delta cycle problems in behavioral modeling by making explicit the event execution order.



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