DOLPHIN INTEGRATION

SMASH 5.8
Mixed signal Diagnosis

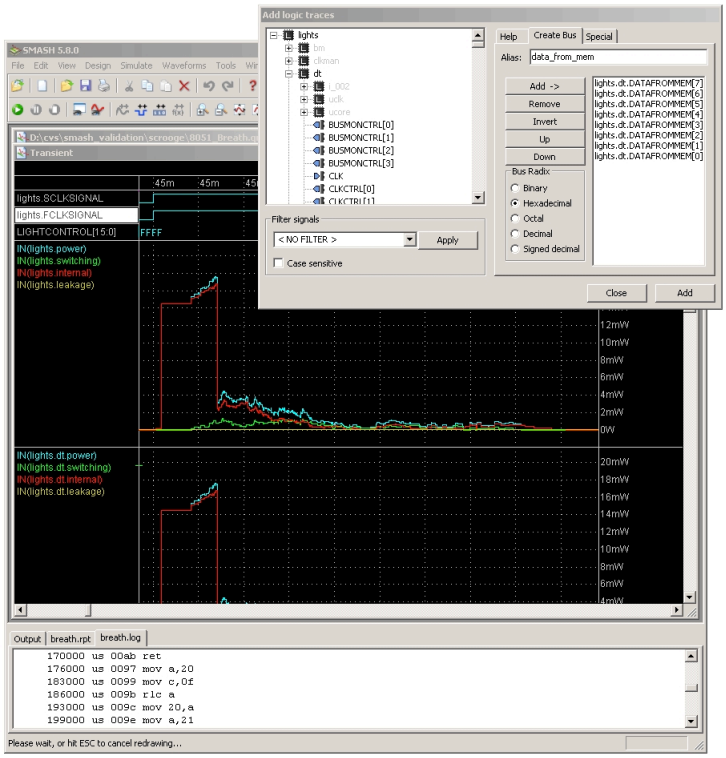
MEDAL

MEDAL Presentation Sheet

SMASH 5.8 extends its capabilities for mixed signal code-coverage and sensitivity-analysis up to detecting flaws in Virtual Testbenches and to identifying circuit weaknesses for the DfM conscious designer. Improvement on the block-busting GUI features facilitate further the adjustments of speed versus accuracy, as well as tracing, now augmented for a hierarchical view applicable to mixed signal design.

KEY ENHANCEMENTS

- Code coverage for HDL-AMS
- DC & small-signal dispersion sensitivity analysis
- Power consumption estimation after Place & Route with SPEF back-annotation
- Enhanced GUI with tree view selection of traces and interactive logging panes
- BSIM4v5 update including a well proximity effect model
- CSDF and VCD output formats for exporting of analog and logic simulation results
- VDA automotive libraries bundled



DESCRIPTION OF THE ENHANCEMENTS

With analysis of sensitivity to dispersion, SMASH provides a fast and accurate solution for the problems of design for yield, manufacturability and robust design of nano-electronic analog circuits. Compared to Monte Carlo analysis, the sensitivity to dispersion is thousands of times faster. Furthermore, the sensitivity to dispersion analysis provides the contribution of each component to the total dispersion, thus design debugging becomes trivial.

As SCROOGE enables power consumption analysis before Place & Route, the SPEF back-annotation now provides it with parasitic capacitance back-annotation for an accurate power consumption analysis after Place & Route. Parasitic capacitances are taken into account to back-annotate the Liberty wire load model. This allows to consider the exact routing capacitance both for cell interconnection wires and for clock trees, which represent an important part of the consumed power.

For increased interoperability, simulation results can now be exported into standard VCD (Verilog Change Dump) format for logic or CSDF (Common Simulation Data Format) for reuse in all compatible EDA solutions. Of course, SMASH can also import and display VCD or CSDF results as well as.

SMASH is available identically under Linux, Solaris and Windows.

Dolphin Integration
Meylan - France
Tel. (33) 4 76 41 74 06
Fax. (33) 4 76 90 29 65

Dolphin Integration GmbH
Duisburg - Germany
Tel. (49) 203 306 2250
Fax. (49) 203 306 2269

www.dolphin-integration.com
smash@dolphin-integration.com

SMASH
HDL-AMS Code Coverage

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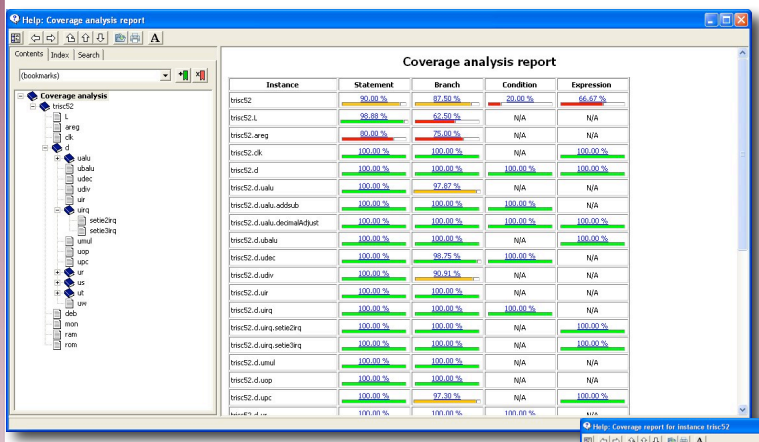
Virtual Testbench exhaustivity is of prime importance for validating circuit designs. HDL-AMS code coverage objectively improves results obtained with unitary tests by providing an immediate measure of tested code completeness.

Designers improve their test development productivity thanks to a clear view of code coverage status allowing to track undetected bugs by identifying untested portions of HDL code and to optimize Testbench development with coverage measurements. It can be done at an early stage in the flow for code execution check. Verification can then be complemented by signal coverage, the toggle test already provided by SMASH, which allows to associate a coverage method to different design levels.

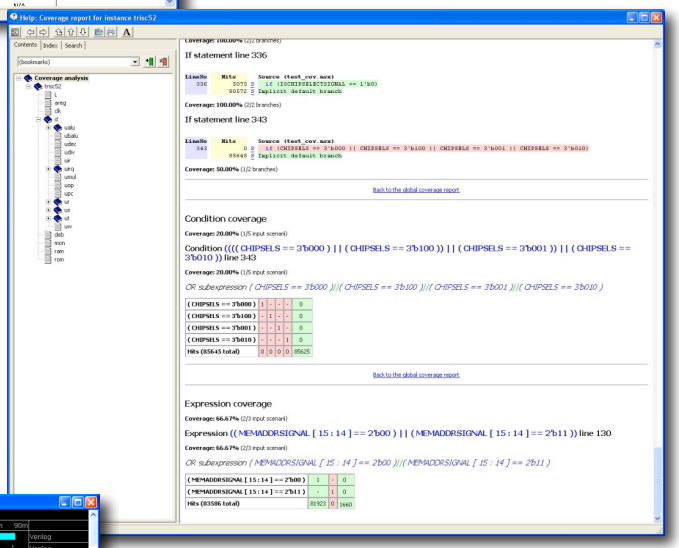


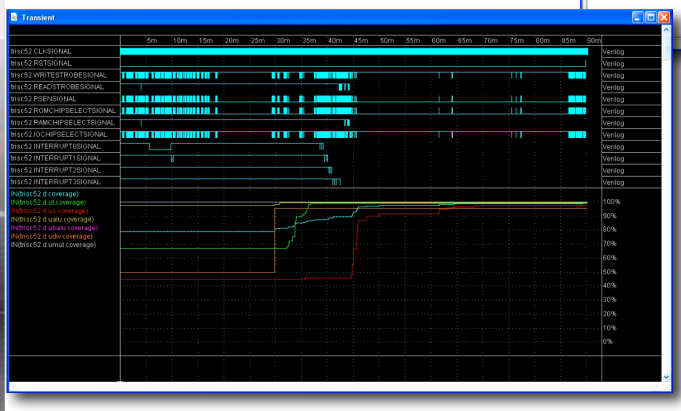
Global reports give an overview of the design's coverage for statements, branches, conditions and expressions as well as links to more detailed analyses.

HTML reports make it easier to navigate analysis results and share them with the rest of your design team.

Detailed reports help figuring exactly where coverage problems are and how to write test cases to solve them.

Hit timing keeps track of when each statement, branch, condition or expression has been hit making it easy to figure out which part of the testbench is useful to cover a specific functionality of the design.





Dynamic coverage with interactive display of waveforms helps create smaller test cases and schedule virtual tests for shorter simulation durations in order to provide optimal verification for each component in the design.

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