# SMASH 5.7
# Empowered Mixity

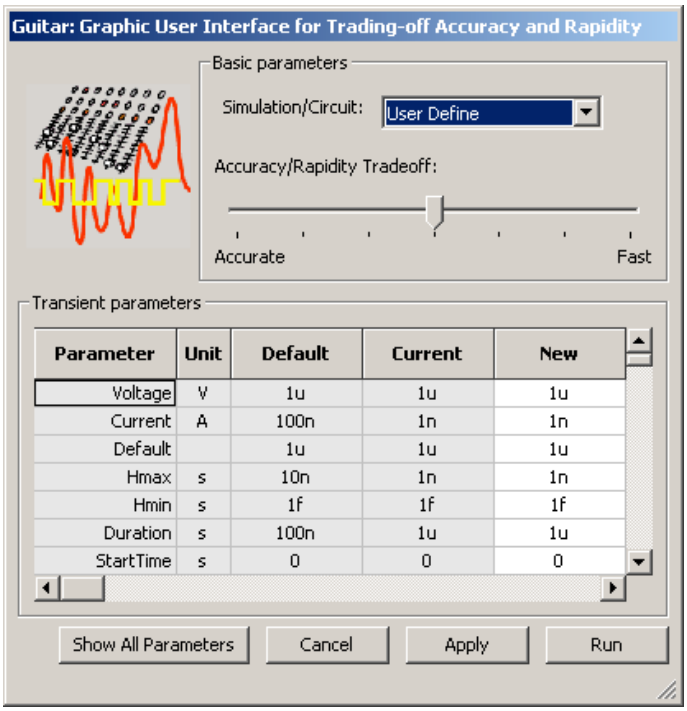
MEDAL Promotion Sheet

SMASH 5.7 is loaded with innovative features which contribute to increasing the productivity of logic, analog and mixed signal designers. With good estimates of power consumption in logic circuits, designers can make an educated selection of low-power architectures and of logic blocks.

**Now, for the first time, a simulator popularizes the setup of parameters to obtain the appropriate speed / accuracy tradeoff for a given Virtual Test.**

## KEY ENHANCEMENTS

- Graphic User Interface for Trading-off Accuracy and Rapidity (GUITAR)
- Logic power consumption estimation (SCROOGE)
- Extended compliance with Verilog-AMS and VHDL-AMS standards
- Unleashed SPICE and VHDL-AMS mixity allowing any hierarchical instantiations
- Enhanced API including script capabilities using Tcl
- Automatically documented SPICE device models
- Increased logic simulation speed (up to a factor of 2)




## HIGHLIGHTS ON NEW CAPABILITIES

Addressing the issue of simulation parameter setup, GUITAR provides an innovative graphical approach to setting the parameters thereby increasing designer awareness to simulator settings and their correlated effects. With the capability to select the appropriate trade-off designers shall detect design bugs faster prior to extract characteristics at the needed accuracy with the highest possible speed:

- The SCROOGE add-on estimates logic power consumption of RTL netlists using standard cell libraries associated with Liberty technology library files.
- Already sporting the best VHDL-AMS compliance on the market, SMASH 5.7 goes further and provides enhanced HDL-AMS compliance, while offering full hierarchical mixing of SPICE with VHDL-AMS.
- Any arrangement of SPICE sub-circuits and VHDL-AMS architectures can be mixed in the hierarchy with improved reporting of AMS node values both in the operating point file and in the simulation results.
- Scripting and extending SMASH is enhanced with Tcl scripting capabilities and an extended Application Programming Interface (API).

**SMASH is available identically under Linux, Solaris and Windows.**

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# SCROOGE
# for Power Consumption

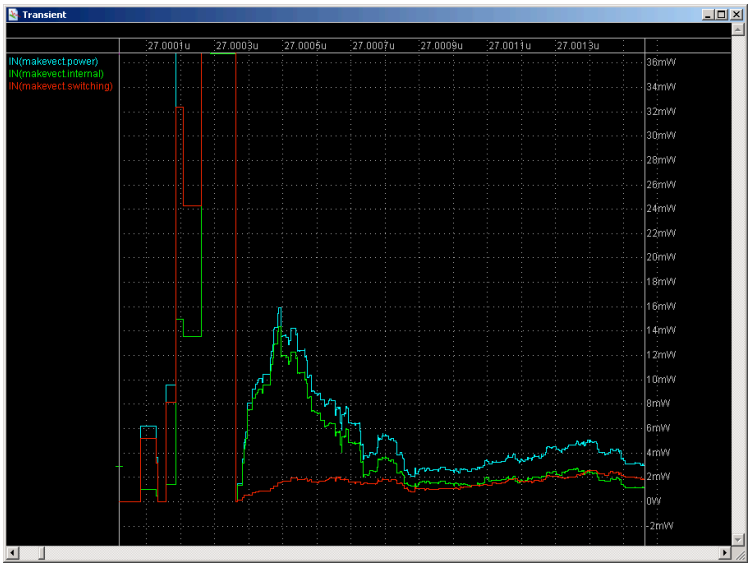
MEDAL Promotion Sheet

The development of portable devices with high performance and multiple features, combined with the arrival of nanometer technologies, makes SoC power consumption a critical point which designers have to deal with during the whole development. The analysis of power consumption has to be performed at the earliest stage in the development flow, so that designers may anticipate potential issues and adapt the architecture with no need for backtracking.

**Keep control of the power consumption all along the design chain with SCROOGE.**

## KEY FEATURES

- Simulate power consumption hierarchically
- Quantify power consumption of RTL designs using Liberty technology library files
- Emulate the clock trees and their power consumption before Place & Route
- Display the leakage/dynamic power consumption during the transient simulation
- Identify critical points (peak)
- Display interactively




## PRODUCT DESCRIPTION

SCROOGE is an add-on to all ASIC options of SMASH, empowering the only true mixed signal simulator with capabilities to simulate power consumption.

Thanks to the use of standard inputs such as the Liberty format (.lib) to define power models, Verilog or VHDL standard cell models, clock tree emulation and a friendly graphic user interface, SCROOGE enables to estimate the power consumption of any logic circuit before layout and to adapt its architecture accordingly.

- Hierarchical evaluation of power consumption of logic blocks, be it within a logic or a mixed signal design, to trigger design improvements.
- Designers can quantify power consumption, track and detect any hot point and optimize it thanks to the link with the synthesizer for selecting standard cells.
- Designers can quantify power consumption of peripherals and optimize application programs thanks to its link with SUCCESS™.

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