Verilog-AMS joining VHDL and SPICE in SMASH 5.6

As the market is moving to nanometer technologies, the critical issue of transient noise takes a new urgency due to the sensitivity of analog and mixed-signal circuits, and even pure logic circuits. This is of course the case for PLL or oscillator designs, but also for evaluating the impact of noise injected by logic onto analog circuits.

SMASH 5.6 eases the practice of transient noise analysis, while leveraging model specific noise equations such as TSMC specific equations.

KEY FEATURES

- STI stress equations for BSIM3/ BSIM4 family of models including both Berkeley and TSMC specific equations
- Enhanced DSP toolbox for periodic signal characterization with jitters measurements and histograms
- Streamlined transient noise analysis, taking into account custom equations and parameters for noise
- Batch-mode data-extraction on FFT results
- Verilog-AMS small signal analysis
- Analog operators in Verilog-AMS such as transition filters, slew integrators or circular integrators
- Enhancement of time control for Verilog timing checks and VHDL VITAL

ViC Disturbances Rejection

The success of SoC Integration of a mixed-signal ViC is unpredictable when high resolution analog or high accuracy logic is involved. SoC integrators are forced to waste at least 2 or 3 test silicon cycles. This “fail & retry” methodology leads to severe losses in performance and in yield, not to speak of costs, both direct (mask and engineering) and indirect (time to market and profit margin). The pragmatic approach needed, mingling Top-Down and Bottom-Up processes, has been developed through the use of DGP models (Disturbance Generation and Propagation). With its mixed-signal multi-level and multi-language kernel, SMASH provides the efficient solution for assessing and measuring the resilience of mixed signal Virtual Components to whatever disturbances injected by the Rest-of-SoC.

To know more about DGP models and our 3 available packages (TIDE™, CHIDE™, CHIMES™), please contact us at: smash@dolphin-integration.com

SMASH is available identically under Linux, Solaris and Windows.

MEDAL promotion sheet

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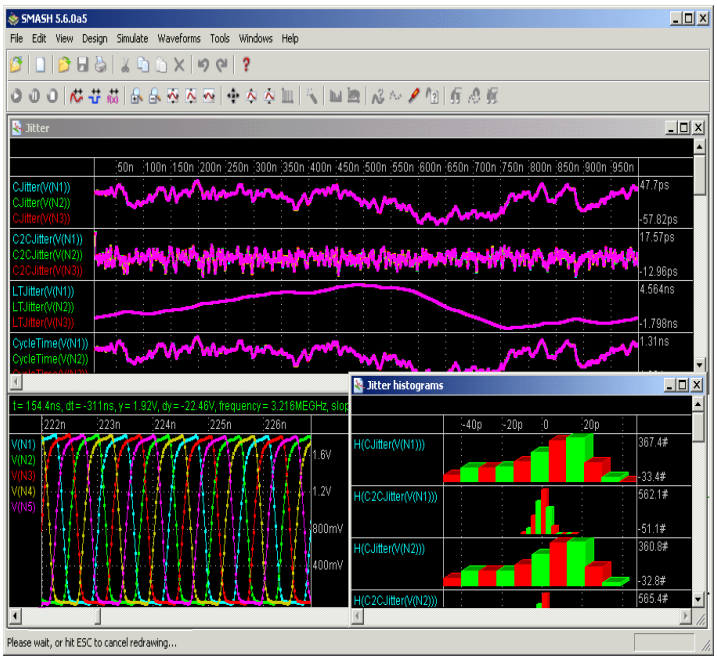
A breakthrough in Jitter analysis with SMASH 5.6

MEDAL promotion sheet

Due to the ever-lasting need for performance improvements, mixed signal designers face the challenge of simulating ever more accurately the effect of jitters in embedded Virtual Components (ViC) such as PLLs or DLLs. Unpredictable Jitters degrade systematically the expected performances of the whole System-on-Chip and, even worse, may induce drastic losses of design yield, down to making a System-on-Chip totally non-functional, unless you can benefit from SMASH 5.6.



KEY FEATURES

Measuring on transient logic or analog waveforms:

- Cycle jitter versus time
- Cycle-to-cycle jitter versus time
- Long term jitter versus time
- Cycle time versus time
- Frequency versus time
- Histogram and dispersion of cycle jitter
- Histogram and dispersion of cycle-to-cycle jitter
- Histogram and dispersion of long term jitter

JITTER MEASUREMENTS

Jitter evaluation still is a mystic problem in search of efficient solutions. However, our Jitter analysis protocol provides means for simulating the intrinsic jitters (cycle jitter, cycle-to-cycle jitter and long term jitter) and for comparing it with objectives so as to perform its acceptance.

Thanks to the transient noise simulation, all kinds of jitter now can be simulated:

- intrinsic jitter due to the noise of components (transistor, resistor...)
- structural jitter due to the architecture of the design.
- cycle jitter, cycle-to-cycle jitter and long-term jitter is computed from transient simulation result.

Simulating the jitters themselves, as well as the impact of jitters on designs, is turned into a quick and fun task with SMASH 5.6.

SMASH is available identically under Linux, Solaris and Windows.

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