SMASH 5.5
enriched with Verilog-A

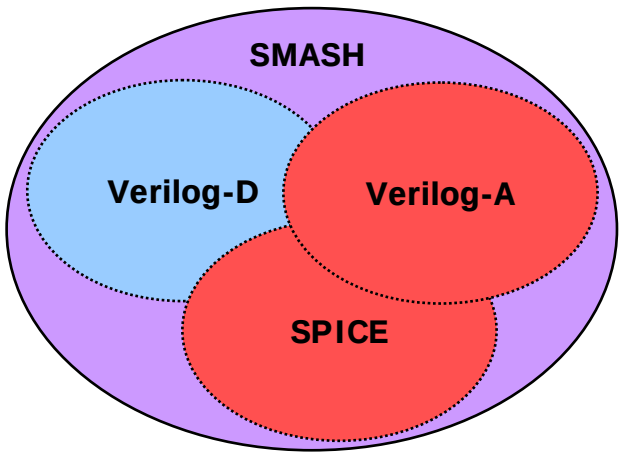
MEDAL promotion sheet

Verilog-AMS benefits designers by allowing them to describe and simulate analog and mixed signal designs using a top-down design methodology as well as the traditional bottom up approach. Moreover, Verilog-AMS provides powerful structural and behavioral modeling capabilities for systems in which the effects of, and interactions among, different disciplines like electrical, mechanical and thermal are important.

SMASH 5.5 extends its natively mixed-language and mixed-signal single kernel to Verilog-A with seamless hierarchical mixing with SPICE.

KEY FEATURES

- Verilog-A for micro-electronic designs
- Mixed SPICE-AMS hierarchical circuit descriptions
- Compiled Verilog(-AMS) models for IP protection
- Automatic dependency handling and library recompilation as needed
- Tracing of Verilog variables
- Verilog-95, 2001 & AMS compliant parser with Verilog-2001 compatible preprocessing
- Command Line Interface (CLI) to Verilog-AMS compiler ready for future batch scripts



Seamless mixing for efficient multi-level calibration

DESCRIPTION OF THE COMPLIANCE

In addition to already supported description languages, a Verilog-A subset targeting micro-electronic designs is now supported by SMASH. This subset supports mixed-signal multi language transient analysis of conservative and signal flow systems with:

- Natures, disciplines and nets
- Analog signals and contribution statements
- Time derivative and integral analog operators
- `@cross` monitored event
- Environment parameter functions
- Standard definitions of disciplines & constants

Furthermore, SMASH provides natural use of library statements (.LIB) for specification of Verilog and Verilog-A libraries of modules. Dependency handling is completely automatic, thereby freeing the designer from manual recompilation of modified descriptions. Furthermore, the compiled “black-box” modules can be used directly and even delivered pre-compiled, for instance for evaluation purposes, thereby providing IP protection.

SMASH is available identically under Linux, Solaris and Windows.

www.dolphin-integration.com
smash@dolphin-integration.com

Dolphin Integration
Meylan - France
Tel. (33) 4 76 41 74 06
Fax. (33) 4 76 90 29 65

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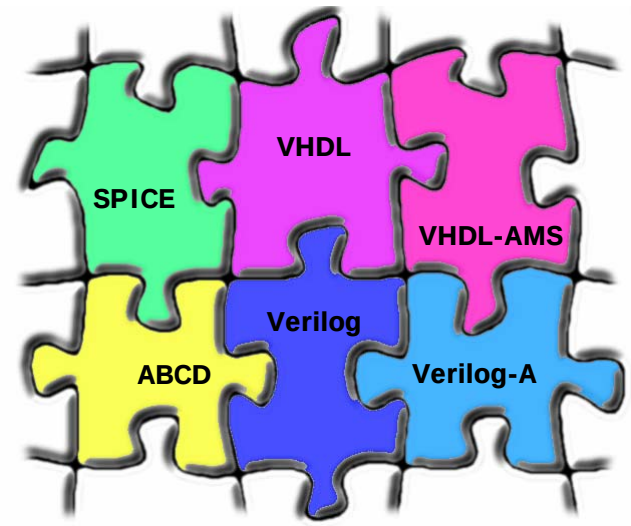
Dolphin Integration GmbH
Duisburg - Germany
Tel. (49) 203 306 2250
Fax. (49) 203 306 2269

SMASH
Mixed Language AMS

The Analog and Mixed-Signal (AMS) extensions for the standard Verilog and VHDL logic Hardware Description Languages (HDL) enable a high-level behavioral approach to mixed-signal modeling and simulation. AMS extends the syntax and the semantics of Verilog and VHDL to allow the description of any type of analog behavior, including mechanical and electro-mechanical systems, and is particularly suited for the description of testbenches.

KEY FEATURES

- Technology independent representation of circuits
- Easier exploration of tradeoffs for different circuit architectures
- Ideal and non-ideal modeling by inclusion of non linearities
- Design reuse at behavioral level
- Creation of reference simulation results for calibration
- Multi language hierarchical circuit descriptions



Mixed-signal multi language single kernel

MODELING FLEXIBILITY & MIXITY

Verilog-AMS, as well as VHDL-AMS, is suitable for the description and simulation of analog, and/or mixed logic/analog systems at several abstraction levels, such as functional, behavioral, macro model, and device levels, and provides the means to:

- verify the entire system at the specification level to allow better architecture and IP selection,
- define analog behavioral descriptions that encapsulate high-level behavioral and structural descriptions of systems and components,
- perform behavioral mixed-signal modeling as compared to transistor-level SPICE modeling,

This allows circuits to be represented at higher levels of abstraction, enables creation of the system earlier in the design cycle and reduces simulation time.

With SMASH, Verilog-A models can naturally be mixed with SPICE, Verilog, VHDL, VHDL-AMS and ABCD models. Complete hierarchical instantiation is provided allowing designers to:

- instantiate Verilog(-A) modules with a SPICE syntax in a SPICE sub-circuit,
- instantiate SPICE sub-circuits with a Verilog syntax in a Verilog(-A) module,
- mix structural Verilog models with behavioral Verilog-A models,
- mix any Verilog description level with SPICE transistor level descriptions.

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www.dolphin-integration.com
smash@dolphin-integration.com

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Fax. (33) 4 76 90 29 65

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Duisburg - Germany
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