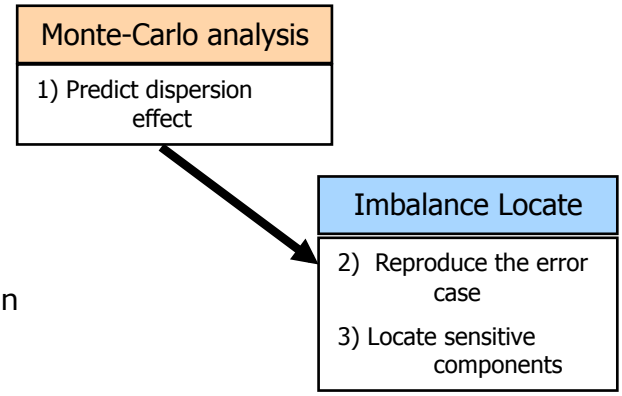
SMASH News:
Features of SMASH 5.3

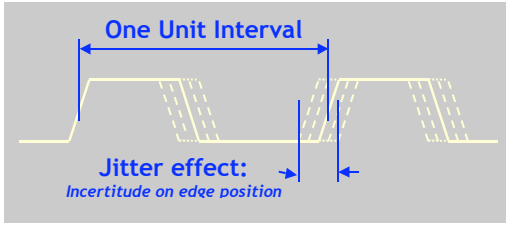
promotion sheet

Due to the ever-lasting need for performance improvements, mixed signal designers face the on-going pressure of time-to-market and of cost reduction. The main improvements provided in SMASH 5.3. are focused on increasing designers' productivity for optimizing the reliability and yield of complex circuits.

Key features:

- Localization of sensitive components causing yield losses
- Fast and accurate simulation of all three forms of Jitter
- Acceleration of pure logic simulation
- HSPICE compatibility
- Interface with LabVIEW™
- Improvements to mixity between languages
- Speed optimization of mixed-signal simulation





Current concerns in mixed-signal design

Random dispersions related to transistor matching, offset dispersion as well as unpredictable Jitter, systematically degrade the expected characteristics and yield of analog circuits.

Two major troubles with available solutions

On the one hand, the well-known Monte Carlo method is useful for predicting the effects of random dispersions, but it is too cumbersome. For optimizing a circuit with respect to analog characteristics and yield, it misses help to diagnose the reason why a given draw would drive to bad performances.

On the other hand, Jitter can be simulated at the electrical level of SPICE classically by means of transient noise analysis or harmonic balance, while operating at a functional level is required for efficiency. Transient Noise analysis is practical only for cells limited to a small number of transistors, due to time and memory consumption, and Harmonic Balance analysis is limited to simulation of phase noise and long term Jitter.

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Tutorials are available on request

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Innovative solutions implemented :

- ***for diagnosing yield losses***

SMASH embeds a patented solution, based on the implementation of the "Imbalance locate" algorithm, enabling designers to quickly detect in a deterministic way, any device (transistor, resistor…) sensitive to mismatch and to random dispersions. It thus ends-up detecting and correcting any design yield drops in a complex circuit.

- ***for simulating accurately all forms of Jitter***

Combined with an innovative analysis protocol for optimal accuracy, SMASH is almost 400 times faster for simulating all forms of Jitter than any simulator relying only SPICE-like transient noise methods. New features enable a wise combination indicated in a tutorial, to involve transient noise simulation, multi-level modeling with calibration between levels, as well as availability of noise sources, with amazing effectiveness.

Other new features implemented in SMASH 5.3:

- ***composing simulated and captured data by Virtual Instrumentation***

In addition to the current interfaces with some schematic editors and with Simulink™, a new interface is now available avoiding designers to compose data resulting from simulation by SMASH with data capture under LabVIEW™.

- ***improving HSPICE compatibility***

In view of implementing a complete Plug'n Play from HSPICE to SMASH, SMASH now supports new types and syntaxes of voltage and current sources for compatibility with HSPICE netlists.

- ***increasing simulation speed for pure logic***

Implementation in SMASH of a Black Box Binary Custom Interface launched as B3CI *in order to allow loading of precompiled VHDL models with no need for compiling the sources.*

- ***optimizing the mixed-signal simulation engine***

Higher circuit loading speeds are attained for large circuits containing sub-circuits with numerous parameters. It also results in faster simulation of mixed-signal designs involving presence of fast logic, with no accuracy loss.

- ***improving the mixity between languages***

VHDL-AMS units can now be directly instantiated in SPICE sub-circuits enabling a complete mixity of netlist at all hierarchical levels including SPICE, Verilog, VHDL, VHDL-AMS and C.

SMASH Seduction, a new free option with limitations on circuits size, is now available facilitating new users to get acquainted with SMASH.

And soon…

In December 2004, all popular languages of the market will be supported by SMASH thanks to the pending compliance with Verilog-A.

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