Missing EDA Links

SMASH 5.19

DOLPHIN INTEGRATION

Extended modeling and mixed-signal capabilities

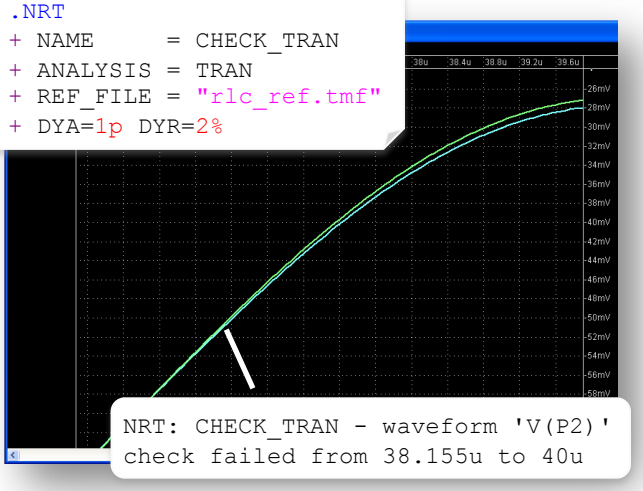
Behind every good simulator there is a good designer! The goal of Dolphin Integration's EDA Solutions and particularly SMASH is thus to improve modeling capabilities and designers' productivity.

SMASH 5.19 provides enhanced features for mixed-signal design including characterization of logic designs with Monte Carlo and Sweep analyses plus an innovative domain coloring viewer to locate and navigate through poles and zeros both in the phase and the magnitude domain.

Key Enhancements of SMASH 5.19

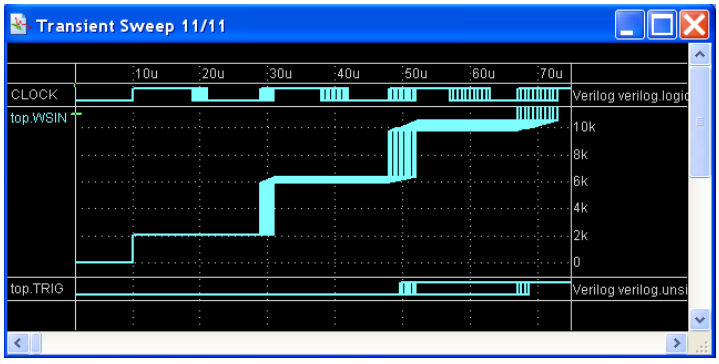
- ✓ Instantiation of behavioral models (HDL/HDL-AMS) in SPICE netlists with mixed macro-models
  - Increased Eldo compatibility using `Y` devices
- ✓ Improved multi-threading capabilities to increase transient simulation speed of analog designs
- ✓ Implementation of Monte Carlo and Sweep analyses on logic designs
- ✓ Capability to reuse logic waveforms (e.g. VCD) as input patterns to decrease overall simulation time
- ✓ Domain coloring viewer with phase and magnitude viewing and zoom in and out functions
- ✓ Support of MM20 model
- ✓ Enhancement of `.SAMPLE` directive when used with noise sources for better accuracy
- ✓ Implementation of `.MODEL` for Verilog-A foundry models
- ✓ Implementation of `.NRT` directive for equivalence checking between waveforms
- ✓ Capability to define a directory to redirect all output files

```
.NRT
+ NAME      = CHECK_TRAN
+ ANALYSIS  = TRAN
+ REF_FILE  = "rlc_ref.tmf"
+ DYA=1p DYR=2%
```



`.NRT` directive

The `.NRT` directive enables to perform equivalence checking by comparing waveforms in order to detect differences. It is useful during technological migration, to compare simulation results from different simulators, to verify the impact of design changes…



Monte Carlo and Sweep analyses on logic signals

SMASH extends the features particularly appreciated by analog designers to the logic world and provides the means to perform Monte Carlo and Sweep analyses on logic signals. This allows making architectural choices by testing the impact of parameter variations (noise, frequency...) or for characterization purposes.

`.SAMPLE` directive

SMASH supports `.SAMPLE` directive to analyze data sampling noise, and to perform noise-folding analysis at the noise output node. SMASH 5.19 improves the accuracy by taking into account all the spikes linked to the noise source.

SMASH is available identically under Linux and Windows

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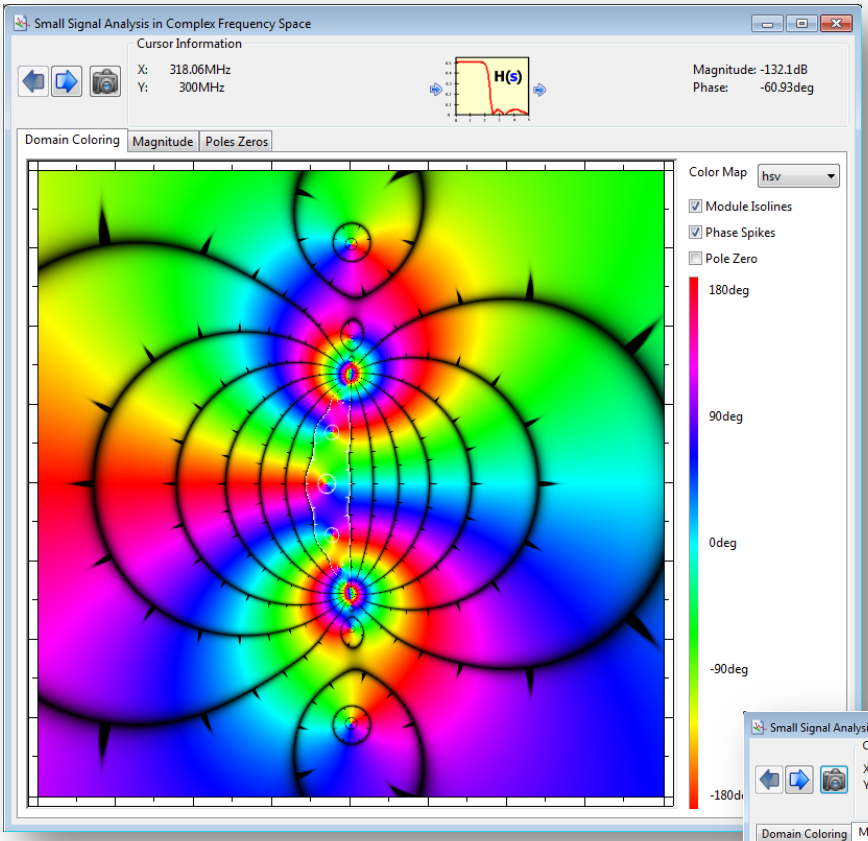
Domain coloring viewer

Domain coloring is a major new feature for analog designers. It allows visualizing the location of poles and zeros in the complex plane, and analyzing their influence on the transfer function as well as on the stability of the system. It also allows generating a Laplace model representing the transfer function for behavioral simulation.

SMASH 5.19 brings to needed flexibility with a dedicated viewer enabling to navigate through poles and zeros and visualize them either in phase or in magnitude.



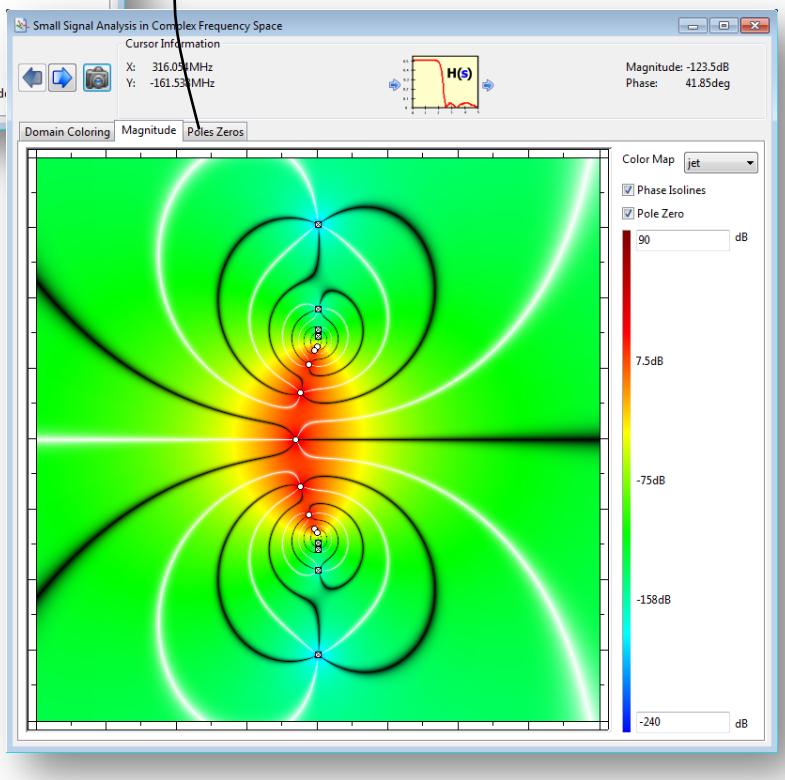
Domain coloring

This is the phase view of the small signal simulation in the complex plane. Count how many times the circle crosses red lines and deduce the order of the pole or zero!

You can zoom in or out, browse the history or generate snapshots.

Poles and Zeros

Visualize the list of poles and zeros, and export Laplace models for behavioral simulation.



Magnitude

This is the magnitude view of the small signal simulation in the complex plane. A thermometric color map allows determining the locations of poles and zeros. In red the poles and in blue the zeros.

Reminder

Domain coloring is available whatever the analog description language (SPICE, Verilog-A or VHDL-AMS).

SMASH is available identically under Linux and Windows