Missing EDA Links

SMASH 5.17

DOLPHIN INTEGRATION

Selective modeling and simulation

Selective modeling and simulation at different abstraction levels requires that simulation performance and accuracy trade-offs be taken into account. It is not possible to give a general recommendation on which level of abstraction should be used, or which performances or effects should be modeled. All abstraction levels have useful applications depending on the specific performance(s) to be verified.

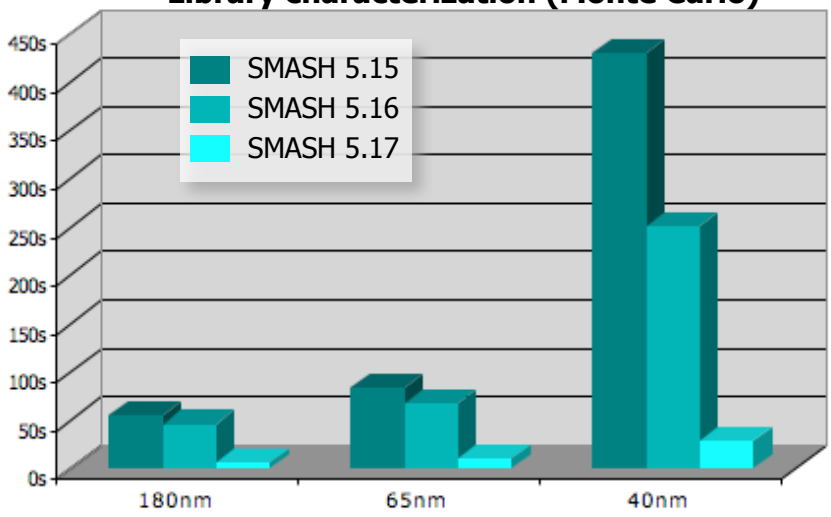
SMASH 5.17 focuses on delivering new features to improve modeling capabilities while still increasing the computation speed.

Real Valued Modeling (RVM) consists in creating models which can be simulated with event-driven logic using mostly floating point values, so-called real values, instead of with analog resolution of real quantities. Real values are continuous as in analog, but time is discrete as in logic. Real Valued Modeling provides new modeling capabilities, in addition to mixed-signal approaches or pure logic modeling of analog blocks.

KEY FEATURES

- ✓ Extended Assertion-Based Verification capabilities
  - Implemented support of System Verilog Assertions (SVA)
  - Property Specification Language (PSL) assertions for designs with multiple clocks
- ✓ Implemented Verilog-AMS `wreal` compliance to enable Real Valued Modeling (RVM)
- ✓ Increased Verilog-HDL and Verilog-A language compliance
  - Analog output variables and indirect contributions
  - Logic tran gates and disable statements which are used in libraries
- ✓ Improved SPICE modeling flexibility and SPICE flavor compatibility
  - `.IF`, `.ELSIF`, `.ELSE`, `.ENDIF` conditional generate statements allow parameter values to affect the structure of a model
  - `.TRACE`, `.PRINT`, `.MEASURE`, `.IC` and `.NODESET` directives inside sub-circuit descriptions
- ✓ Enhanced `.ALTER`, `.MEASURE` and `.MULTIOP` directives
- ✓ Increased designers' productivity by accelerating circuit loading as well as Monte Carlo and sweep simulation

Library characterization (Monte Carlo)



SMASH 5.17 delivers substantial simulation speed improvements for analyses with multiple runs, such as Sweep, Alter and Monte Carlo.

The graphic on the left shows that the Monte Carlo simulation time for a library characterization has been divided by 10 with 40 nm foundry model parameter sets.

SMASH is available identically under Linux and Windows.

dolphin-integration.com/eda
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SMASH 5.17

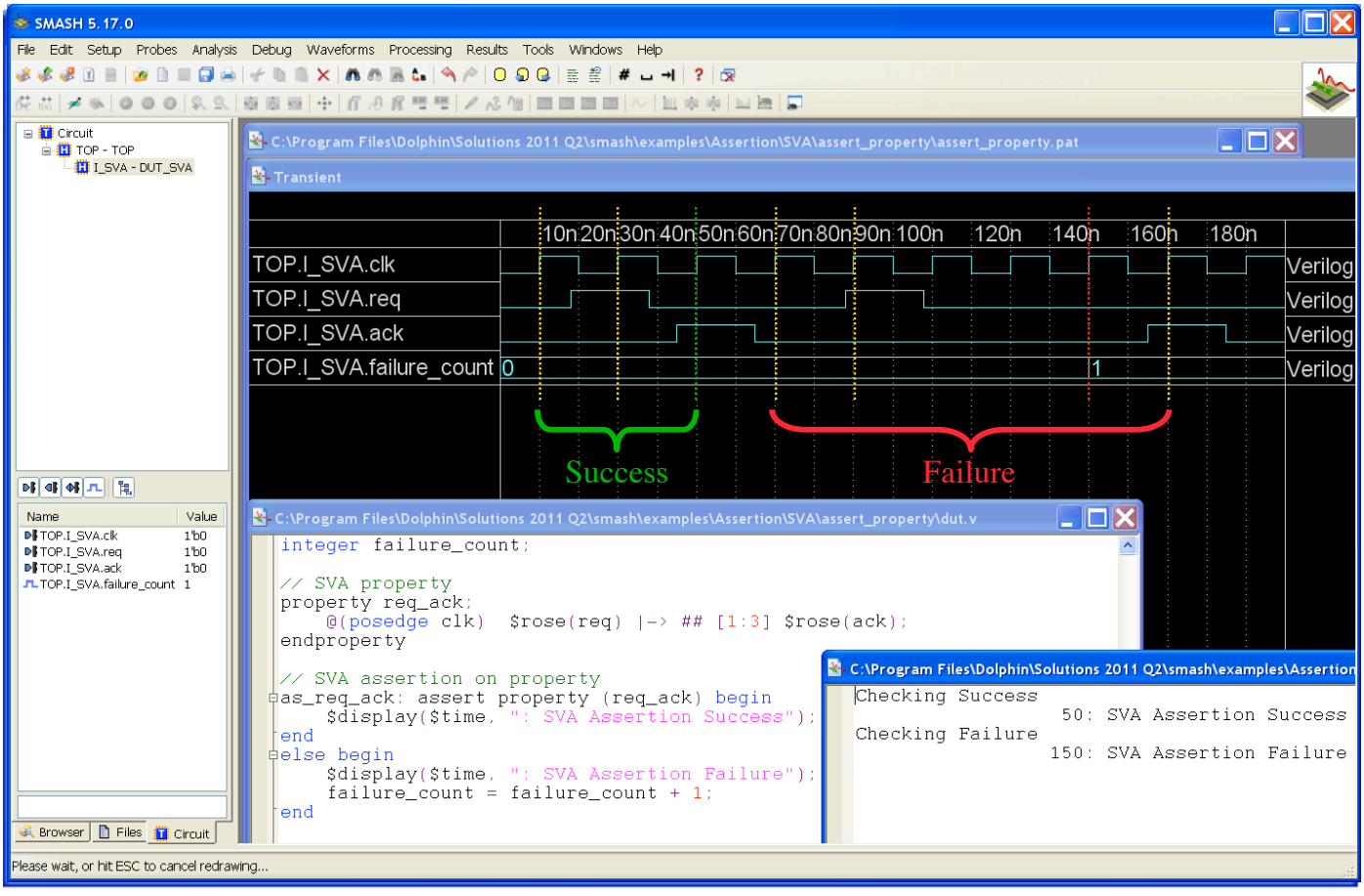
DOLPHIN INTEGRATION

Assertion-Based Verification with SMASH

SMASH 5.17 provides state-of-the-art support of SystemVerilog Assertions (SVA) with which designers can verify complex temporal properties using immediate and concurrent assertions.

Assertions are an integral part of the design and verification process and are becoming more and more popular as designers' learn the required skills. Such verifications are based on temporal properties (either in SVA or in PSL) describing the expected behavior of a design. In much fewer lines of code than corresponding VHDL or Verilog verifications, assertions facilitate the verification process by helping designers detect hard to find bugs through analysis of simulation results.

SVA is one step ahead of PSL as it is totally embedded into the SystemVerilog language. This implies that assertions can be an integral part of SystemVerilog designs and testbenches, instead of just observers. Therefore, SVA allows to use design local variables, as well as to react easily on property verification successes or failures.



TIMA Laboratory - Techniques of Informatics and Microelectronics for integrated systems Architecture
SVA and PSL properties simulation based on the HORUS technology developed by the Verification and Modeling of Digital Systems (VDS) group at TIMA - http://tima.imag.fr/vds.

SMASH is available identically under Linux and Windows.