Missing EDA Links

SMASH 5.16

DOLPHIN INTEGRATION

Compliance

Speed

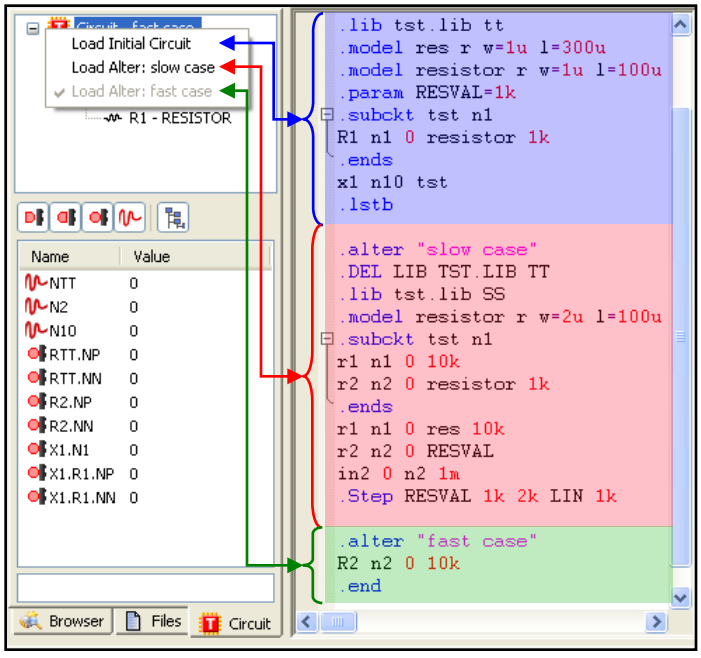
Ease of Use

State-of-the-art analog and mixed-signal design requires analysis capabilities allowing to automate and secure multiple design steps while simplifying the investigation and debug of mixed-language designs. While the circuit browser gives direct access to instances and models in the netlist, error and warning messages issued by SMASH now contain clickable file and line number information for efficient debugging.

SMASH 5.16 delivers new analyses dedicated to analog design, along with Verilog/Verilog-A behavioral improvements both for logic testbenches and for analog modeling.

KEY ENHANCEMENTS

- ✓ Increased analog design productivity with linear loop stability (.LSTB) and data sampling noise (.SAMPLE) analyses
- ✓ Improved compliance with Verilog standards for testbench descriptions
- ✓ Increased Verilog-A simulation performance including support of analog functions for behavioral modeling
- ✓ Extended HSPICE compliance with the support of .ALTER and .DEL LIB directives
- ✓ Enhanced debugging capabilities with direct access to analog ports in the “circuit” pane
- ✓ Improved device analysis capabilities with interactive editing of SPICE device parameters and drawing of device characteristics



Alternate netlists using .ALTER

DESCRIPTION OF THE BENEFITS

- Verilog compliance enhancements target testbench descriptions with access to signals and variables using hierarchical names and system tasks for file access in read mode.
- Verilog-A improvements include additional capabilities for behavioral modeling, with user defined analog functions and string parameters for modules, as well as increased simulation performance, more specifically for Compact Models.
- Error, warning and information messages issued during the parsing of SPICE descriptions have been significantly enhanced in order to provide the designer with more easily exploitable messages with explicit file and line number information. The file and line number in the message is interpreted by SMASH as an active link which allows to quickly locate the origin of problems simply by clicking on the link in the report.
- The “circuit” browser has been extended to provide quick access to the source level description of instances and models directly from the user interface of SMASH.

HIGHLIGHT

Don’t miss out discovering the new “**ICD – Interactive Curve Display**” solution for waveform viewing.

SMASH is available identically under Linux and Windows.

Dec-2010

Missing EDA Links

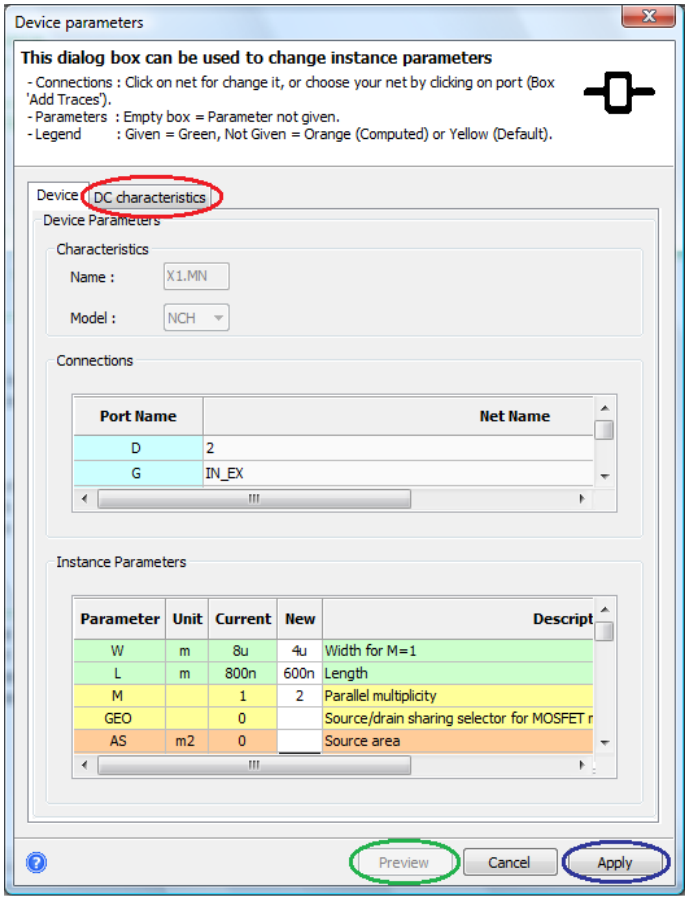
SPICE Device Characteristics

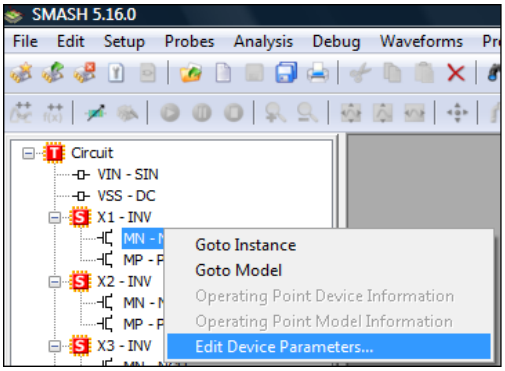
DOLPHIN INTEGRATION

Device Parameters

DC Characteristics

Preview Sources





SPICE DEVICE PARAMETERS

From the *Circuit Browser* pane in the SMASH user interface, interactively update SPICE device instances: edit instance parameters and change port connections.

For instance, the MOS transistor “MN” in sub-circuit instance “X1” has been updated:

- width: 8u -> 4u
- length: 800n -> 600n
- multiplicity: set to 2

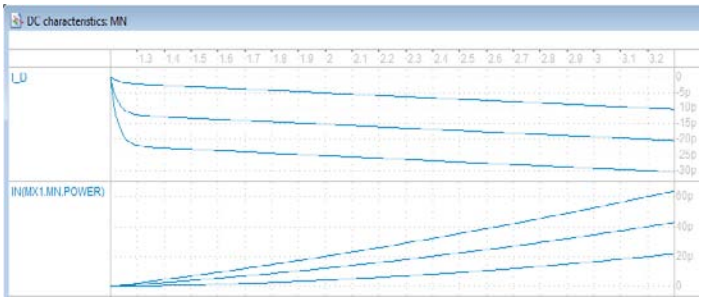
The **Apply** button adds a `.SUBSTITUTE` directive to the simulator control file with new SPICE device syntax:

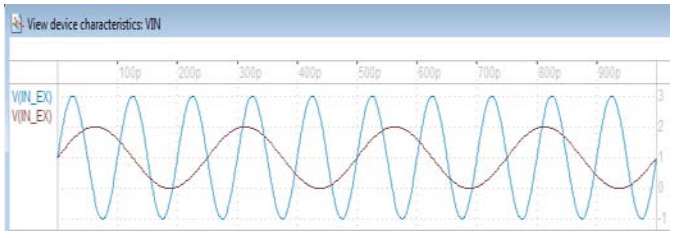
```
.SUBSTITUTE X1.MN 2 IN_EX 0 0 NCH W=4U L=600N M=2
```

DC CHARACTERISTICS

The **DC Characteristics** tab is useful to check and study the behavior of edited devices by tracing DC Characteristics.

Any instance output parameter (current, voltage, transconductance...) can be traced versus any input parameter.





PREVIEW SOURCE WAVEFORMS

When SPICE voltage or current sources are edited, the source waveform can be directly traced, via the **Preview** button. This is useful to check the source behavior before running a simulation.

SMASH is available identically under Linux and Windows.

Dec-2010