Missing EDA Links

SMASH 5.15

DOLPHIN INTEGRATION

Interoperability

Compliance

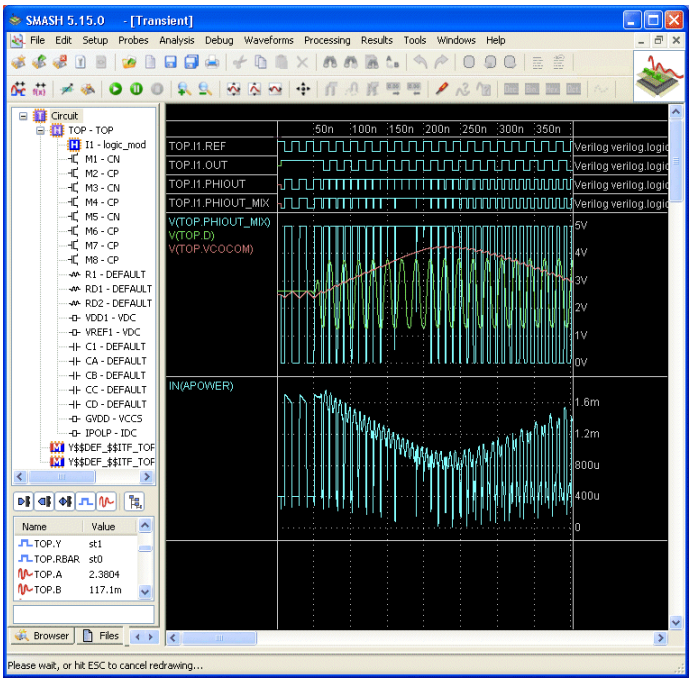
Speed

As the complexity of circuits increases, the time required to perform verifications explodes, especially when using a traditional full SPICE, so-called full-chip, approach. The only viable solution is to use a multi-level approach where parts are modeled at higher abstraction levels, with equivalence checking to ensure appropriate accuracy of behavioral models, in order to speed-up complete circuit or system simulations.

SMASH 5.15 delivers major speed and capacity improvements along with mandatory analog equivalence checking: a must for analog behavioral modeling!

KEY ENHANCEMENTS

- ✓ Analog equivalence checking with measures and template checking on waveforms (transient, FFT, small-signal, Jitter...)
- ✓ Improved compliance with Verilog standards (including partial Verilog 2001) paving the way for System Verilog compliance
- ✓ Increased circuit size capacity for Verilog, both gate-level and RTL, and Verilog-A descriptions, including Compact Models
- ✓ Accelerated circuit loading and transient simulation of Verilog and Verilog-A models
- ✓ Increased compatibility with HSpice foundry files using the GEOSHRINK directive for device dimension scaling
- ✓ Increased circuit size capacity for SPICE when using statistical foundry models



DESCRIPTION OF THE BENEFITS

- Analog equivalence checking features enable top-down and bottom-up verifications as well as verification of integration rules (refer to second page for a more detailed description).
- Integration of a new third-party Verilog family language parser has enabled improving language compliance with Verilog-HDL, Verilog-2001 (such as ANSI port declarations, localparam, "@*" statements...) and Verilog-A.
- Embedding of a new in-house logic and analog behavioral simulation technology has enabled reducing the memory footprint and improving simulation performance. Applied to Verilog-HDL and Verilog-A, circuit loading time has been divided by 10 for Verilog circuits and the simulation engine is two times faster.
- For future releases, the language parser and simulation technology open the road to VHDL 2008, System Verilog and Verilog-AMS compliance, as well as mixed-signal (Verilog/VHDL, logic/analog) performance improvements (loading and simulation speed, circuit size capacity).

TUTORIALS

Don't miss out discovering the new "**FFT Basics**" tutorial.

SMASH is available identically under Linux and Windows.

Jun-2010

Missing EDA Links

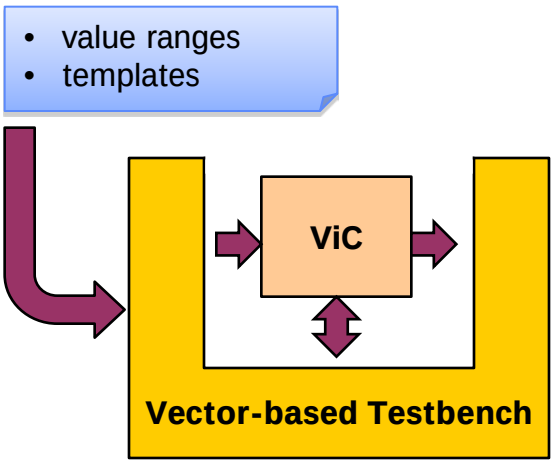
Analog Equivalence Checking

DOLPHIN INTEGRATION

Top-Down

Bottom-Up

Integration Rules

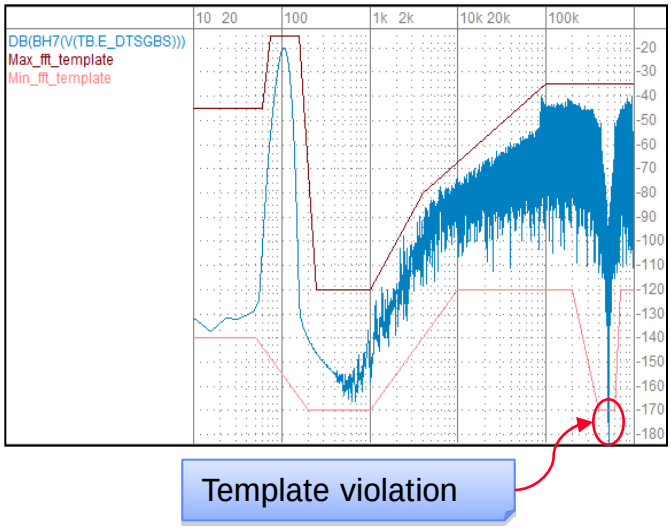


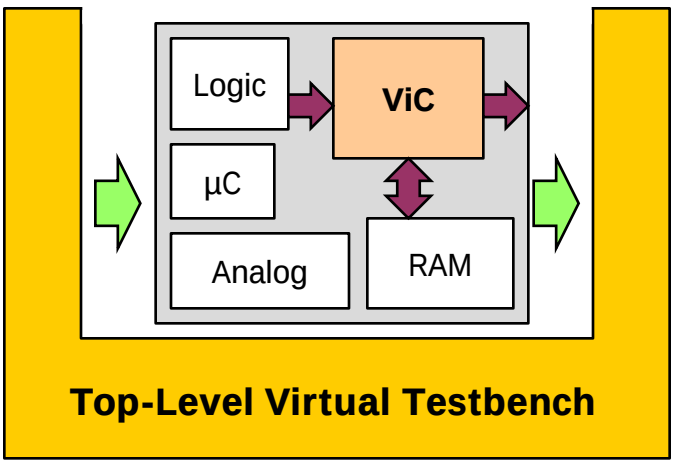
TOP-DOWN EQUIVALENCE CHECKING

A typical example of top-down analog equivalence checking is to check that the implementation of an analog or mixed-signal cell or block matches its specification. A specification is generally a collection of value ranges or templates. Thanks to its unique set of measure statements, SMASH can easily perform this ascertainment of equivalence and validate an implementation whatever the analysis: transient, FFT, small signal, noise, dc...

BOTTOM-UP EQUIVALENCE CHECKING

A typical example of bottom-up equivalence checking is for proving that a behavioral analog model of a cell or block is equivalent to its implementation. In this case, the implementation level simulation (SPICE) is the reference from which the template files are captured. The template files are then used to verify the equivalence of the behavioral analog model.





INTEGRATION RULES

Embedding an analog or mixed-signal Virtual Component (ViC) in a SoC requires checking the integration rules of the ViC. Respecting these rules is crucial to maintain the ViC performances after integration. Checking these rules generally consists in verifying that the rest of SoC output (profile) matches a template. For example, the jitter characteristics of a PLL, or the SNR of a CODEC is guaranteed if, and only if, the spectrum on the power supply voltage remains inside a given template.

SMASH is available identically under Linux and Windows.

Jun-2010