Missing EDA Links

SMASH 5.14

DOLPHIN INTEGRATION

Interoperability

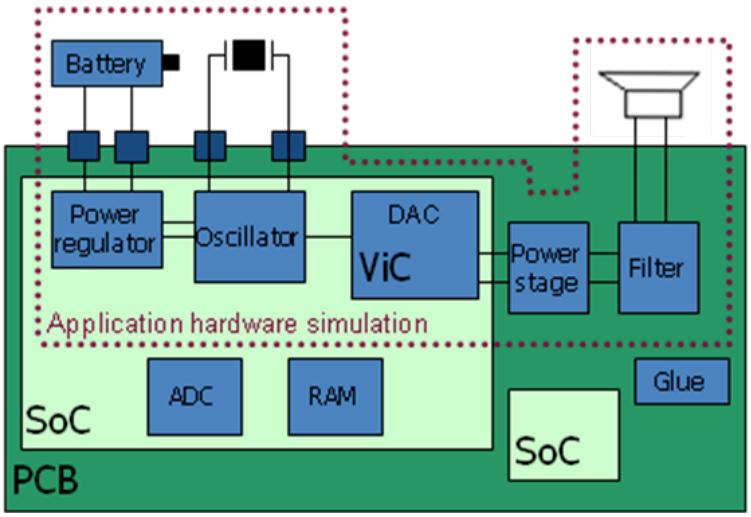
Compliance

Speed

The Application Hardware Modeling (AHM) approach consists in checking an overall function performed jointly by parts of the system, comprising some Virtual Component (so called ViC or silicon IP blocks) within a SoC assembled on the PCB with discrete components, such as Quartz, PMIC, or MEMS, along with application software. Assembling such Application Schematics (ASC) requires compliance with a variety of models at different description levels in order to perform complete multi-level, up to multi-domain, and mixed-signal design performance verifications.
SMASH 5.14 delivers major enhancements for designer productivity!

KEY FEATURES

- ✓ Increased compliance with SPICE and foundry model parameter sets through parameter order independent elaboration
- ✓ Up to ten-fold acceleration of the loading of large circuit descriptions in SPICE
- ✓ Ten-fold acceleration of the loading of large HDL-AMS descriptions (up to 10 times in Verilog-A and 100 times in VHDL-AMS)
- ✓ Enhanced mixed-language capabilities with instantiation of SPICE devices directly in Verilog-A descriptions
- ✓ Extended compliance with the PSL (Property Specification Language) language
- ✓ Improved support for the Laplace transform in VHDL-AMS, Verilog-A and SPICE
- ✓ Integration of HiCUM v2.23 bipolar model



Application Schematic assembled using the models of each element at the appropriate description level

DESCRIPTION OF THE ENHANCEMENTS

- Assertion-Based Verification capabilities have been extended through increased PSL compliance with support for all sequence operators and enhanced support for complex SEREs.
- SPICE devices and sources can be instantiated directly in Verilog-A modules, in compliance with annex E of the Verilog-A language reference manual. Designers can now easily mix SPICE level structural descriptions into Verilog behavioral descriptions.
- SPICE parsing has been upgraded to separate the circuit netlist parsing phase from the circuit elaboration phase in order to speed-up circuit loading and pave the way for more elaborate handling of the circuit description in characterization iterations. As a result, circuit parsing is more compatible with traditional SPICE simulators: parameter instantiation is now independent from the netlist order for better compliance with foundry model parameter sets. Warning and error messages also contain file and line number indications.

TUTORIALS

Don't miss out discovering the new "Application Hardware Modeling" and "Audio Files" tutorials.

SMASH is available identically under Linux and Windows.

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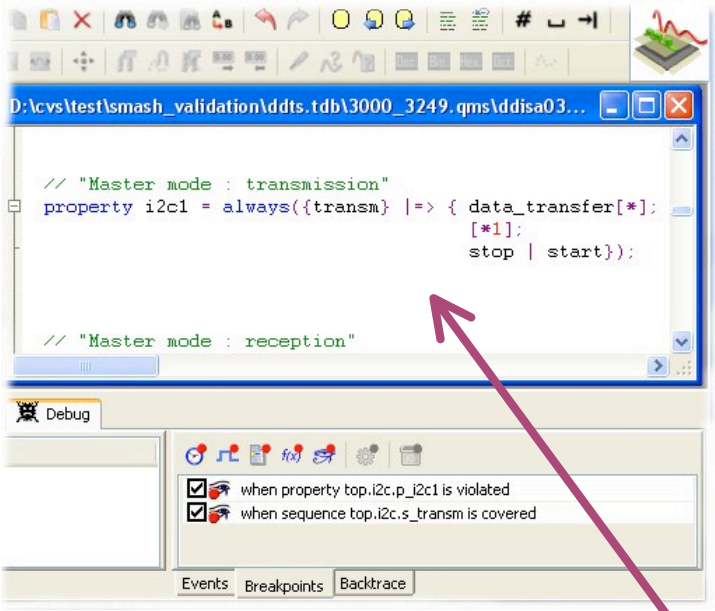
Assertion-Based Verification

DOLPHIN INTEGRATION

Property Assertions

PSL

Sequence Coverage



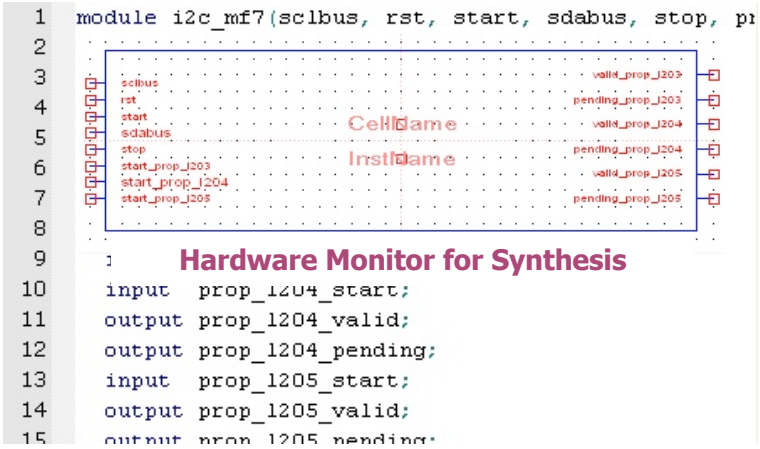
Relevant options of SMASH include native support for simulation of **PSL** (Property Specification Language) properties, both **assertions** and **coverage**, with very low time and memory overhead.

The integration of PSL is complete with source code syntax coloring, association of verification units with Verilog or VHDL models or instances, logging of PSL assertion violations, reporting of PSL sequence coverage results, and breaking into the source level debugger for investigation of design defects.

The **SLED-SDG** option enables conversion of PSL assertions into synthesizable RTL models. This makes it possible for the designer to automatically integrate PSL verification units into a Design Under Test in an FPGA for emulation or in a testchip. Embedding hardware verification units in prototypes increases verification speed by several orders of magnitude.

Automated generation of synthesizable models from PSL assertions can also be used as an efficient alternative to writing safety related parts of a design directly in RTL. These hardware verification units are integrated for embedded monitoring.

Verification Unit for Simulation



Hardware Monitor for Synthesis

TIMA Laboratory - Techniques of Informatics and Microelectronics for integrated systems Architecture

PSL properties simulation based on the HORUS technology developed by the Verification and Modeling of Digital Systems (VDS) group at TIMA - http://tima.imag.fr/vds.

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