

# Missing EDA Links

## SMASH 5.13

### Interface Devices

### Mixed SPICE & Verilog-A

### Hierarchical Tolerances

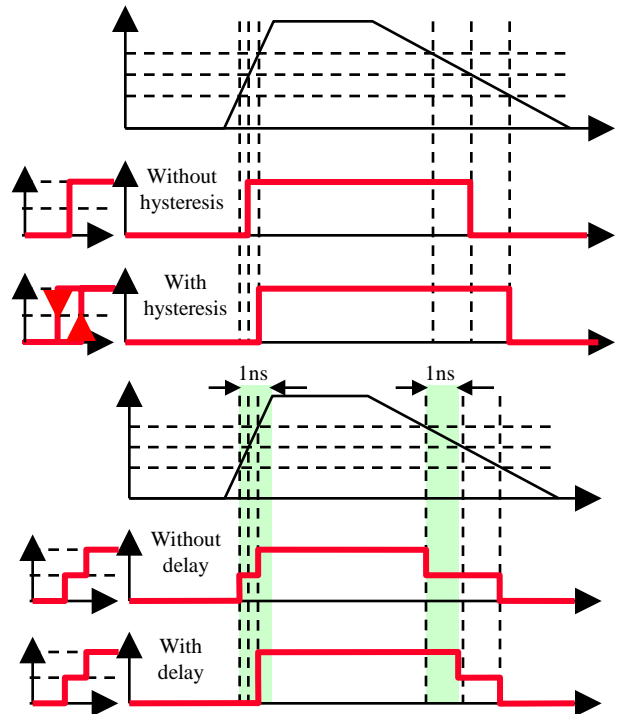
DOLPHIN INTEGRATION

The design and verification of systems, integrating ever more features, increases the complexity of Virtual Tests needed to check whether specifications are met. Multi-level verifications have become mandatory to ensure right-on-first pass designs of multi-domain systems. Each part of the system must be modeled at the appropriate level, with the adequate hardware description language, depending on the required accuracy for measurement of characteristics.

**SMASH 5.13 increases the flexibility for mixing levels of hardware description languages and provides straightforward configuration of hierarchical tolerances.**

#### KEY FEATURES

- ✓ Extended capabilities for mixed-signal interface devices with hysteresis, delay to X, interconnection of multiple logic signals...
- ✓ Flexible hierarchical tolerances on different nets or parts of the circuit depending on the target accuracy and speed trade-off
- ✓ Optimized Verilog-A behavioral model handling with tolerances and multi-processor support
- ✓ Power-Up analysis for mixed-signal circuits
- ✓ Input and output .VEC digital vector files, including HSPICE compatibility
- ✓ Time precision handling for logic and mixed-signal simulations longer than 9223 seconds
- ✓ Verification of PSL properties using the simple subset with mixed-signal extensions
- ✓ Optimized SPICE library parsing for ten-fold reduction of circuit loading time when using statistical model parameter sets



#### DESCRIPTION OF THE BENEFITS

Mixing hardware description languages, such as SPICE, Verilog, Verilog-A, VHDL and VHDL-AMS, for complex SOC Integration, unavoidably entails simulation mixing logic and analog models as well as mixing models at structural and behavioral levels.

- Mixing analog and logic signals requires inserting interface devices for conversion of the signals. The single-kernel engine of SMASH has always delivered push-button mixed-signal simulation with automatic insertion of interface devices. These devices are now enhanced to provide even more flexibility in the control of the conversion with hysteresis, delay to X...
- Multi-level simulation requires handling different accuracy settings for best accuracy versus speed trade-offs. The flexible support of VHDL-AMS tolerances in SMASH has been extended to SPICE and Verilog-A. Tolerances specified by the designer in Verilog-A models are now handled in the same manner as for VHDL-AMS. Furthermore, specific SPICE tolerances can also be specified on different nets or parts of the circuit. Whatever the analog description language used, be it SPICE, Verilog-A or VHDL-AMS, accuracy can be tuned in the hierarchy to help convergence and increase simulation speed.

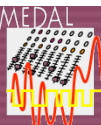


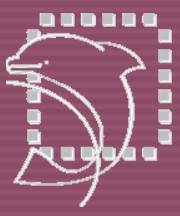
SMASH is available identically under Linux, Solaris and Windows.

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# Missing EDA Links

## SMASH - Interface Devices

Automatic Insertion

Mixed Macro-Models

Connection by Name

DOLPHIN INTEGRATION

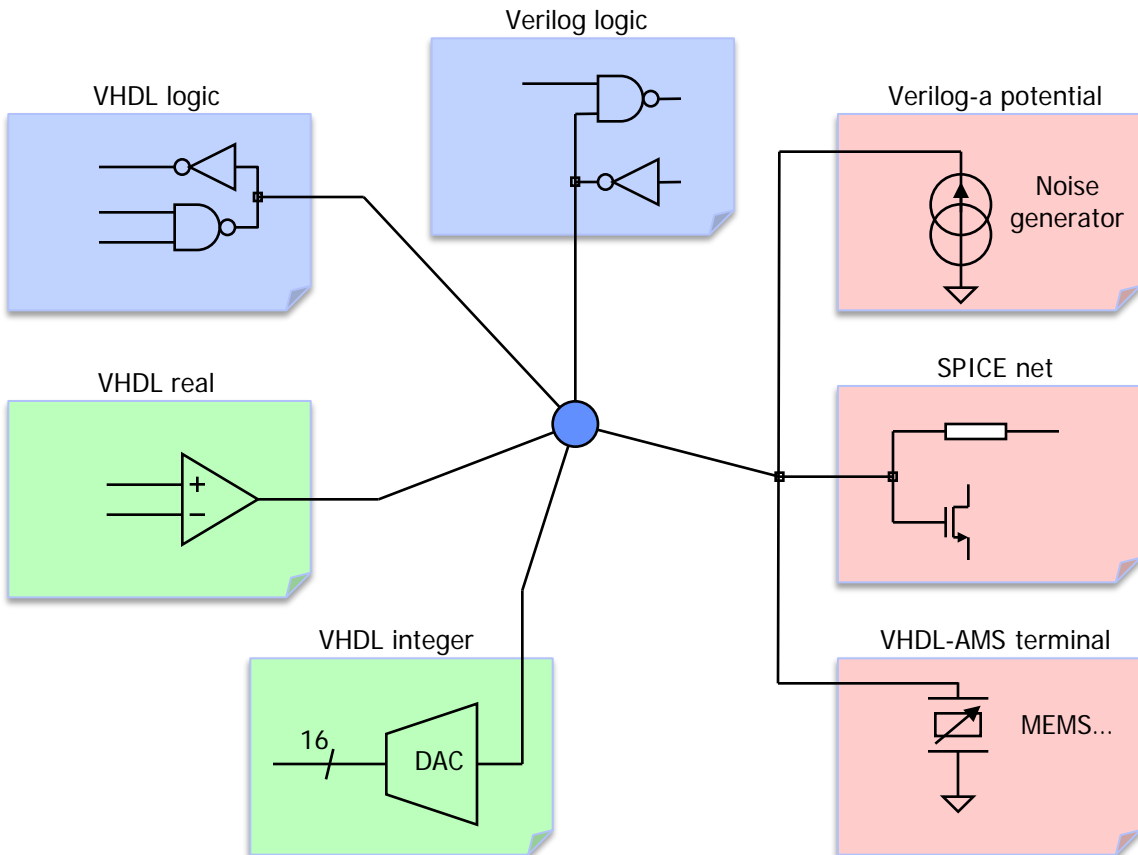
A mixed macro-model is characterized by the fact that its instances can be connected to analog nets and/or logic signals. The foremost mixed macro-model delivered with SMASH is obviously the mixed-signal interface device model. Indeed, the mixed-signal multi language single kernel implemented in SMASH provides native, and, in most cases, totally automatic mixing of analog (SPICE, Verilog-AMS or VHDL-AMS) and logic (Verilog or VHDL) descriptions in the same circuit.

Interface devices are used to link the analog and logic devices. They carry both an analog voltage (continuous) and a logic value (discrete); equivalence schemes are used to translate voltages to logic levels and conversely. Whenever a netlist is parsed by SMASH, interface nets are automatically identified and interface devices are automatically inserted unless the designer has explicitly inserted beforehand interface devices for a finer grain control of the conversions performed at the interfaces.

### INTERFACE DEVICE CAPABILITIES

Mixed-signal simulation setup has never been so flexible and easy. A unique interface device enables simultaneous interconnection of analog nets and logic signals of different natures, with automatic parameterized conversions, allowing mixing of:

- Multiple languages (VHDL, Verilog, SPICE, Verilog-A, VHDL-AMS)
- Multiple net and signal types (std\_logic, real, integer, quantity, potential...)



SMASH is available identically under Linux, Solaris and Windows.

