DOLPHIN INTEGRATION

SMASH 5.12
Increased Speed & Capacity

MEDAL

MEDAL Presentation Sheet

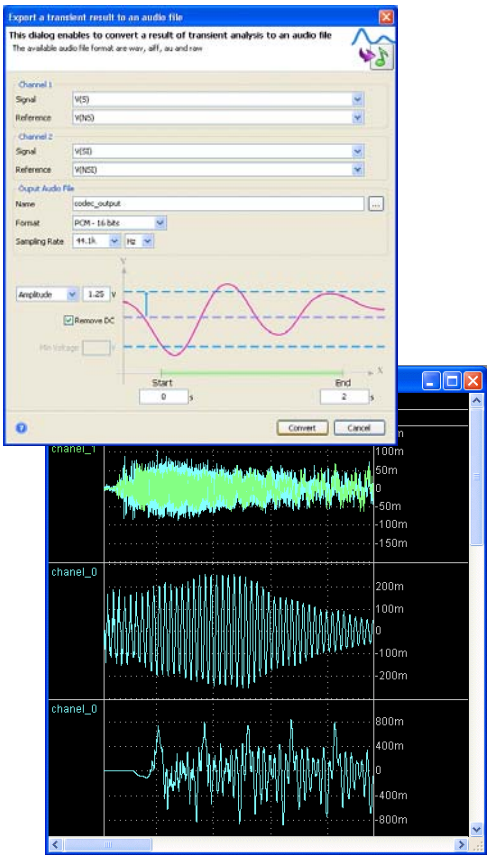
SMASH 5.12 enhances its leadership position with functionalities for Logic and Mixed Signal (LMS) as it now satisfies two crucial requirements for the SoC Integrator:

It provides new circuit monitoring capabilities, akin to real-time "Detectors", leveraging on-line and conditional expressions, supervised by an "Expression Watch Panel"!

It simultaneously provides a significant improvement for the capability of Virtual Testing thanks to Homotopy based heuristics for detection of multiple operating-points.

KEY ENHANCEMENTS

- ✓ Multi-core aware equation evaluation for SPICE device models to speed-up the analog simulation
- ✓ Automatic detection of multiple operating-points to ensure design operation for all bias points
- ✓ Improvement of Virtual Test capability with Homotopy based heuristics for the search of operating-points in addition to existing heuristics
- ✓ Simplified use of audio data files with import to drive analog simulation and for waveform display, and export from transient simulation results
- ✓ Time precision handling for VHDL and VHDL-AMS simulations longer than 9223 seconds
- ✓ Enhanced debugger with expression watches, expression breakpoints and breakpoint actions
- ✓ Verilog-2001 negative timing checks along with increased circuit loading capacity
- ✓ User selection of which SPICE device and model parameters to output to the operating-point file
- ✓ Enhanced find and replace in built-in text editors
- ✓ SPICE flavor compatibility improvements for temperature parameter and nested sub-circuits



DESCRIPTION OF THE EASE OF USE

Enhancing the "detector" capabilities, and on the roadmap towards assertions, the integrated debugger now provides evaluators for expressions which can either be watched or used as breakpoint conditions to monitor circuit operation. Expressions can be composed of signals, quantities, arithmetic and comparison operators, logic operators in Verilog syntax, and common Verilog functions. When watched in the "Expression Watch Panel", they are updated automatically during simulation as well as whenever a pause occurs, whether caused by a breakpoint or by a user request.

Expression Breakpoints will pause the simulation whenever the associated expression becomes true. Breakpoints can be assigned a condition that will cause the breakpoint to be skipped when the condition is false, as well as a counter that can be used as a filter depending on the occurrence count: they serve as "Conditional Detectors". In addition, breakpoints can also be used as "trace points" for non-interactive debugging.

SMASH is available identically under Linux, Solaris and Windows.

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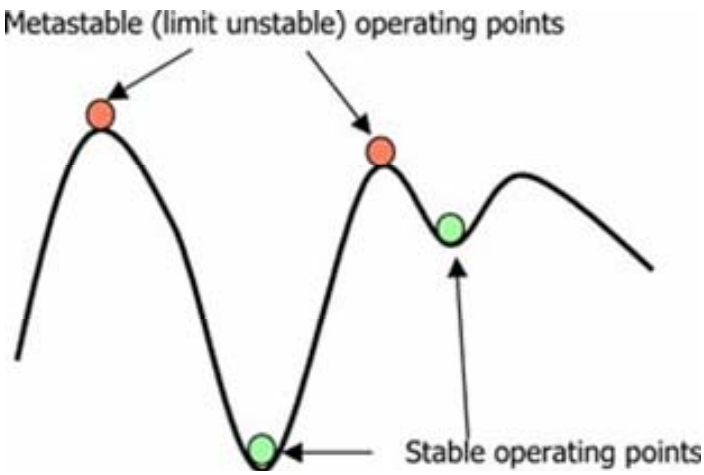
Biasing is the method for establishing predetermined voltages and/or currents at various points of a circuit to set an appropriate operating-point. When biased as designed, the circuit performs as expected. However, multiple alternate operating-points, stable or meta-stable, may exist which render the circuit useless when self-biased with respect to an unintended operating-point. Such situations cannot in general be predicted by inspection of the circuit topology.

SMASH 5.12 instead proposes a capability for multiple operating-point search to overcome these limitations. It can automatically search for and find multiple (in most cases, all) operating-points of a circuit.

The operating-point, also known as "bias point" or quiescent point, is the set of DC voltages and/or currents which, when applied to the circuit, represents a non-ambiguous starting state when applying some input sequence. It is defined by the value of each net voltage and the state of each device for which the circuit is at a "rest state" or steady state.
Several operating-points can exist in analog, logic, or mixed signal circuits much like the various summits and troughs on a mountain range. The saddle points represent meta-stable operating-points.



DESCRIPTION OF THE BENEFITS

Finding DC operating-points is the first and maybe the most determinant design task for both the circuit designer and the SoC Integrator. In most simulators, the DC operating point is found by using Newton–Raphson based heuristics. Such heuristics have two shortcomings that are now overcome:

- Firstly, convergence cannot be guaranteed unless the initial starting point (to be specified by the designer) is sufficiently close to the actual solution. Unfortunately, the designer either may not know the solution or cannot give a sufficiently accurate initial guess. Furthermore, even if the designer could give an accurate initial guess of the required operating-point to cause the circuit to operate as desired, nothing guarantees that self-biasing of the circuit will place it in the desired operating-point!
- Secondly, a single operating-point can be found during each analysis. Neither existence nor even location of other operating points is determined once the heuristics have converged to a particular operating-point.

With the operating-point analysis, SMASH proceeds through a complete search, using all heuristics in sequence, and gives the first stable result that is found. With multiple operating-point analysis, SMASH helps the designer to **determine whether operating points are multiple and to identify meaningful ones in order to simplify eradicating unwanted operating-points** which render the circuit useless when self-biased in such operating conditions!

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