Missing EDA Links

Assertion-based Verification
PSL

DOLPHIN INTEGRATION

The language of bug trappers

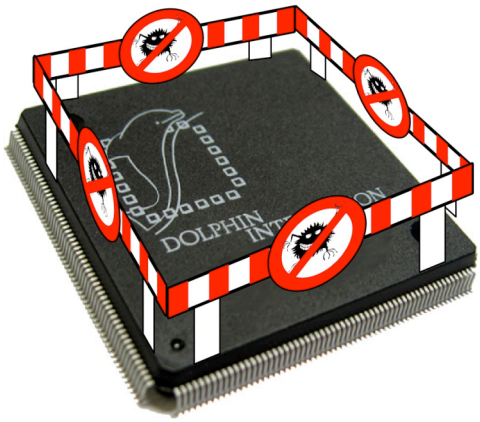
As design verification takes so much of designers' time at the various stages of new product development, the top productivity enhancement solution is that which best helps improve the RoI for quality checks.

Ensuring that the behavior of a design meets its specification from its earliest stage onward, the bundle of Schematic Link EDitor SLED with the mixed-signal simulator SMASH, named SLASH, now allows designers to conveniently perform **assertion-based verification (ABV)**.

PSL (Property Specification Language) targets bugs by tracking properties asserted as Boolean and temporal expressions to describe the expected behavior of the design. SLASH enables simulating such assertions in PSL* for detection of defects all along the design flow. Furthermore, SLED-SDG enables generating synthesizable verification units for embedded error detection logic in the prototype or circuit!

KEY BENEFITS

- ✓ Define the properties and instantiate them in the design: no need to adapt your PSL assertions to the design context!
- ✓ Incorporate RTL synthesizable hardware checkers in the design thanks to automatic generation from PSL assertions
- ✓ It allows to
  - assess the operating conditions of a chip or FPGA
  - be sure of the reliability of a secure circuit or a mission-critical circuit all along its lifespan thanks to self-test and automatic diagnosis assistance



ASSERTION-BASED VERIFICATION

Today, assertions are an integral part of the design and verification process and are becoming more and more of popular use in designers' world. Such verifications are based on temporal properties describing the expected behavior of a design. These properties are checked using assertions, either embedded in the HDL descriptions or as independent protocol checkers. In much fewer lines of code than corresponding VHDL or Verilog verifications, assertions facilitate the verification process by helping designers detect hard to find bugs through analysis of simulation results.

What is needed ? Good assertions defined by the designer and an integrated intelligent debugger plus a solution, such as SMASH, supporting the simulation of assertions.

Besides **dynamic verification of PSL properties** which is supported by SMASH, SLED provides an easy way of integrating and reusing properties, as well as generating synthesizable monitors. Thanks to the option SLED-SDG, such hardware monitors can be used either in hardware emulation **for validation purposes**, or as part of any circuit to **detect dysfunctions in real-time**.

*TIMA technology under UJF/Grenoble INP license

SLASH & SLED-SDG are available identically under Linux and Windows.

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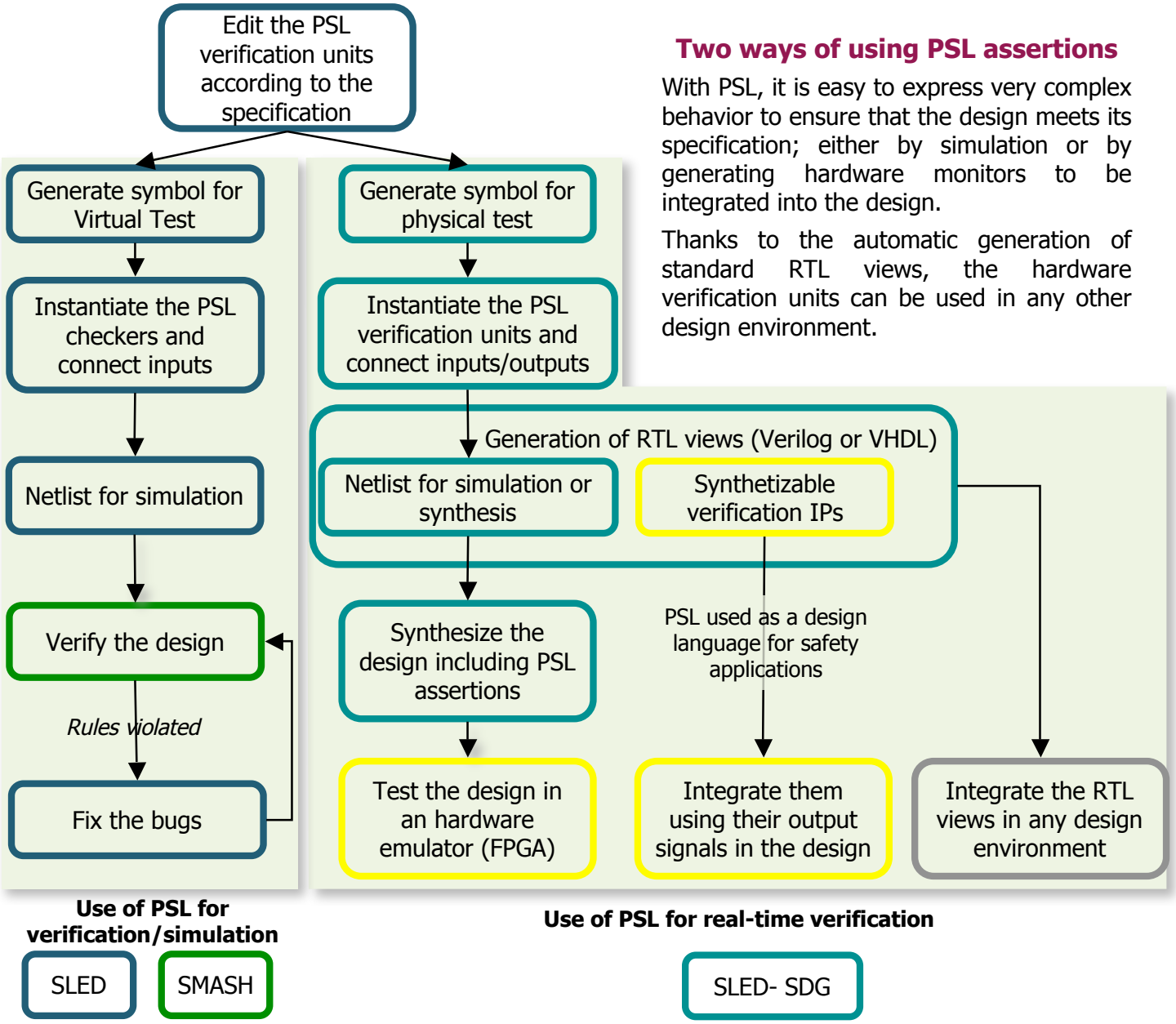
Assertion-based Verification PSL

DOLPHIN INTEGRATION

Securing a design with embedded PSL assertions



Two ways of using PSL assertions

With PSL, it is easy to express very complex behavior to ensure that the design meets its specification; either by simulation or by generating hardware monitors to be integrated into the design.

Thanks to the automatic generation of standard RTL views, the hardware verification units can be used in any other design environment.

Adopt PSL and...

- ✓ Reduce both the time and the cost of your verification process
- ✓ Easily design circuits with embedded monitoring capabilities!

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our free Discovery Options at:
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