DOLPHIN DESIGN

# SLED 3.6 & SMASH 7.6

## SPEED-UP OP/DC and Transient analyses

SMASH 7.6.0 mixed-signal simulator significantly speeds up OP/DC and transient analyses of analog and mixed designs in advanced nodes by a gain between x2 and x6.

These major speed-up gains have been possible thanks to new methods and algorithms without losing simulation accuracy, as merge of identical SPICE instances, improve evaluation of MOS transistors, RC reduction methods and new Solver.

All these features allow SMASH to be as fast or even to overtake the major fastest golden spice simulators, while ensuring accuracy of a single solver SPICE simulator.

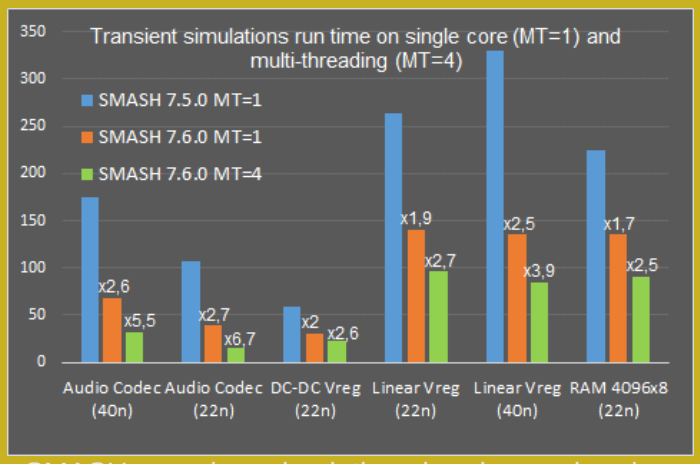
## Reduction RC to speed-up simulations

SPICE simulations with RC parasites are essential in advanced process nodes for realistic and precise simulation results. Parasitic extraction adds large amounts of capacitance and resistance elements to these circuits which significantly increase simulations run time. Thus, to speed-up simulations without losing accuracy, it is crucial to reduce the parasitic netlist size.

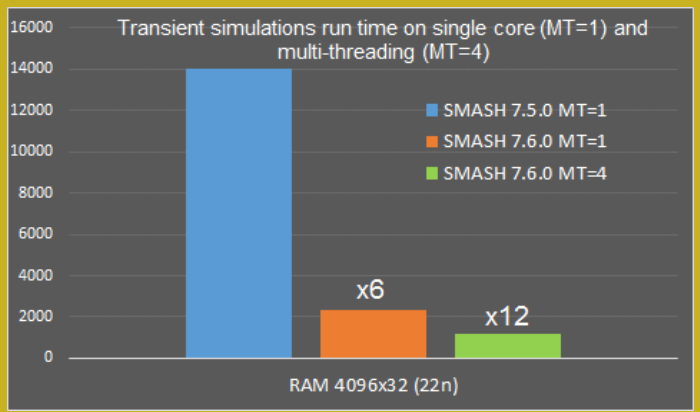
In SMASH, new method based on TICER algorithm has been developed and integrated to speed-up OP/DC and Transient post-layout simulations of circuits with extracted RC parasites.
This method has successfully accelerated simulations of extract RC circuits in advanced nodes with a speed-up gain until x2, without losing accuracy.

## New analog fast parallel solver NICSU

Multi-threading simulations have been considerably speed-up thanks to the use of NICSLU a new parallel fast solver: http://nicslu.weebly.com.
This new solver is faster than the previous one use in almost all cases for mono-threading simulations.
Moreover multi-threading simulations directly provide faster simulations with the same accuracy. Transient simulations can be speed-up from x2 to x2.5 when using CPU with four cores.




SMASH speed-up simulations in advanced nodes.




SMASH speed-up simulation gain thanks to new NICSLU solver and RC reduction method, with 335k capacitors, 32k MOS and 210k resistors

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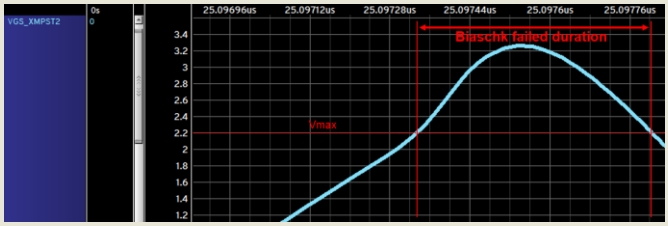
## Support of .BIASCHK directive

In advances nodes circuits simulations, it is crucial to check electrical rules or safe operating area before launching tape-out phase in design process.

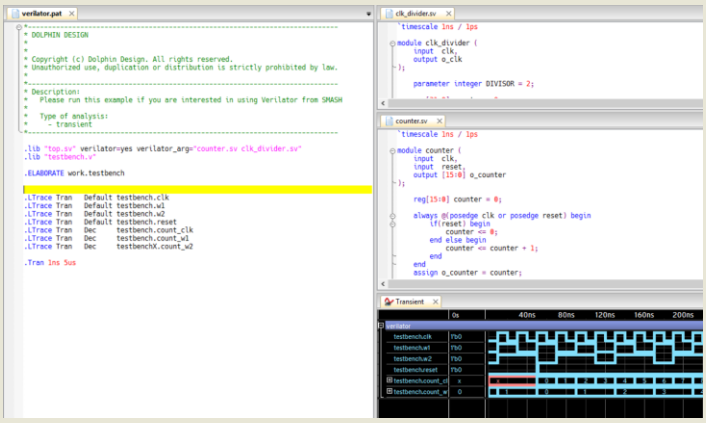
Thus SMASH is now supporting .BIASHCK directive which is commonly used by major semiconductor foundries to check electrical rules on transistor MOS voltages.

.BIASCHK directive is flexible to adapt and to constraint electrical rules for circuits which are, for example, dedicated to general public or automotive.

```
.biaschk subckt mname=nmos simulation=all
+ message="mos: Vgs bias outside limits"
+ min=-2.2 max=2.2 interval=1p terminal1=g terminal2=s monitor=v
```




```
Type=subckt      Terminals=V(XDUT_CIRCUITA_NEVASTANDALONE.XNEVA_ACU.XLSMREF.XMPST2.G)-V(XDUT_CIRCUITA_NEVASTANDALONE.XNEVA_ACU.XLSMREF.XMPST2.S)
time=  25.0973200973u  -  25.0978168266u      peak= 3.26326107551
```



## Support of SystemVerilog

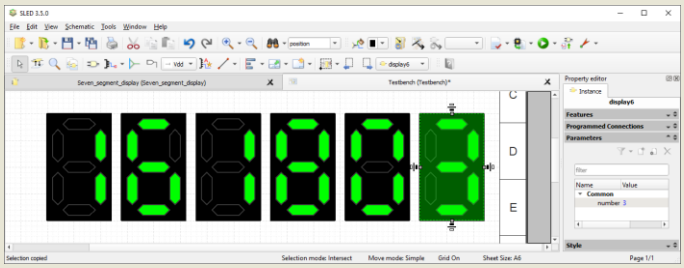
SMASH is now supporting SystemVerilog language for RTL synthesizable simulations, thanks to the integration of Verilator. Verilator is open source Verilog/SystemVerilog simulator. Verilator converts Verilog HDL modules to C++ models which are simulated by SMASH.

Moreover Verilator has good speed-up performance results versus the closed-source Verilog simulators.

For more information, you can consult Verilator website: https://www.veripool.org/wiki/verilator

## SLED improves the user experience by allowing to:

- show/hide instance pin of instance elements in a schematic to simplify the schematic and improve its readability when a pin is optional
- set the color of instance elements in a schematic by TCL script to change the graphical representation of an instance depending on its parameter values
- define tags in parameter definition to bring order when a cell contains tens of parameter
- filter the parameter by tag in the property editor to highlight certain parameters according to their meaning/usage



**YOUR FEEDBACK MATTERS**

To contribute suggestions and requests for the Dolphin EDA Solutions, please provide feedback on your user experience to **support@dolphin.fr**.