SLED 3.2 & SMASH 7.2

NEW CUSTOM STATIC ELECTRICAL RULES CHECKING

SMASH 7.2 provides new API functionalities to scan analog circuit across DEVICE connections and to verify your own custom **Static Electrical Rules Checking**.

An example part of the installation kit enables to detect automatically and quickly all MOS transistors with gates directly connected to supply sources, without launching any simulation.

This is more deeply explained in a new application note.

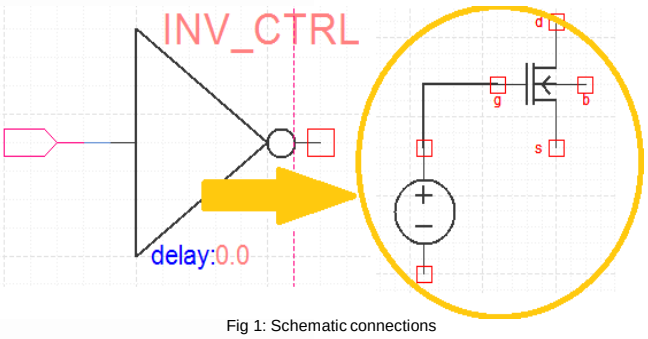

Fig 1: Schematic connections

selector.pat | staticERC.log

```
SERC Supply nets:
  [1]  VDD
  [2]  VSS
WARNING: SERC_CheckMosGateSupply, port G of XI_1.XINV_CTRL.MPQ MOS is dir
WARNING: SERC_CheckMosGateSupply, port G of XI_1.XINV_CTRL.MNQ MOS is dir
WARNING: SERC_CheckMosGateSupply, port G of XI_1.XAND_CTRL_OR_AB.MPA MOS
WARNING: SERC_CheckMosGateSupply, port G of XI_1.XAND_CTRL_OR_AB.MNA MOS
Static Electrical Rules Checking Summary:
  0 error(s) found
  4 warnings(s) found
  1 rule(s) checked
```

Fig 2: SERC report file

IMPROVED SIMULATIONS IN ADVANCED PROCESS

Analog simulations convergence is improved and sped up for the advanced **FINFET and FDSOI process technologies**.

- Simulations of transistor with low values access resistors (less than 10µA) have been accelerated without any trade-off on the accuracy of the results.
- Convergence of recent HISIM HV v2.1 MOS transistor model used in advanced process has been improved.

IMPROVED HDL LANGUAGE SUPPORT

Verilog-A:
SMASH 7.2 supports probabilistic system functions, genvar loop (for) variable in analog block and access functions on net array elements in order to simulate complex Verilog-A models.

SystemVerilog:
SMASH 7.2 supports « always_ff », « always_comb » and « always_latch » processes, packages, real array initializations and declarations in generate constructs.

SPICE MODEL UPDATE

BSIM-BULK v106.2:
BSIM-BULK (formerly BSIM6) is the new Bulk MOSFET model from the BSIM Group. The model provides excellent accuracy compared to measured data in all regions of operation. It is already used in last 40nm process technology.

EKV v2.6:
The EPFL-EKV v2.6 model has been reviewed and updated in order to provide complete documentation of the parameters and to trace parameters and internal variables for any analysis type.

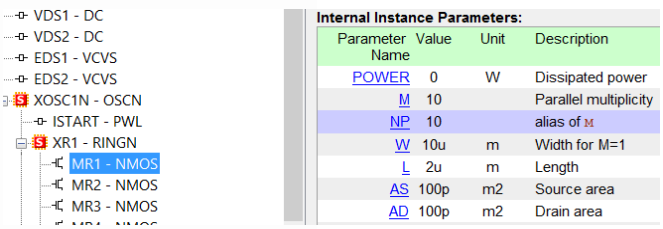

Fig 3: Access to EKV parameters

SLED 3.2 & SMASH 7.2

ENGAGE MIGRATION OF SLED PARAMETERS

For preparing the migration towards a future release of SLED which will allow multi-level schematics, SLED 3.2 will detect the incoming incompatibilities like parameter definitions inside a project, a library, a symbol or a schematic.
In future releases of SLED, parameter definitions will only be allowed in the cells. Parameter definitions detected in projects, libraries, schematics or symbols will then be automatically migrated into cells.

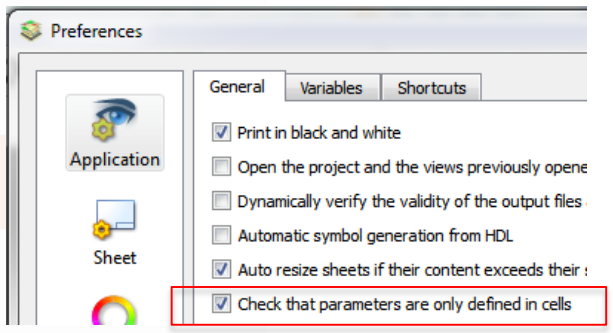

Fig 4: SLED application preferences

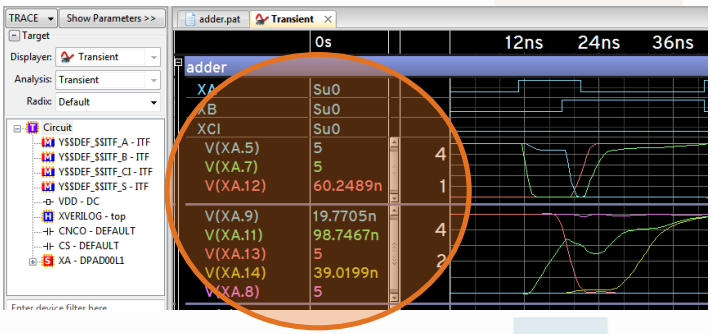

Fig 5: Increased font in SMASH waveform viewer

CHANGE TEXT FONT SIZE IN WAVEFORM VIEWER

SMASH 7.2 and ICD 2.2 provide a new option to enable the font size changes in the waveform viewer.

Indeed, you can improve the readability according to your needs (display resolution, projection, documentation…)

USER FEEDBACK & SUPPORT REQUEST

SLED 3.2 and SMASH 7.2 help you report your feedback about the products and send your support requests.

The Welcome page as well as the Help menu provide an easy access to preformatted emails addressing both purposes.

Do not hesitate to report your remarks, comments or suggestions. Your feedback will help us improve the future releases of EDA Solutions.

YOUR FEEDBACK MATTERS

To contribute suggestions and requests for the Dolphin EDA Solutions, please provide feedback on your user experience to **support@dolphin.fr**

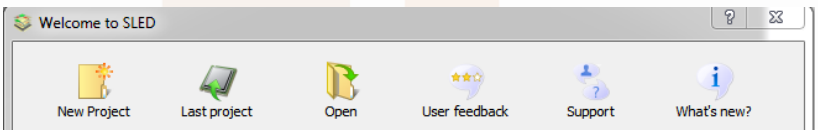

Fig 6: SLED Welcome page

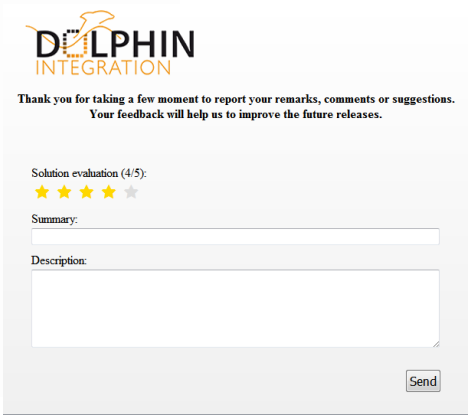

Fig 7: SLED user feedback