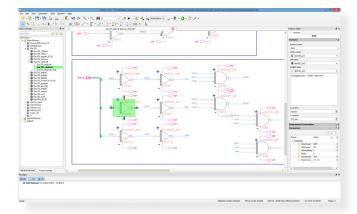


SLASH IN THE LENS

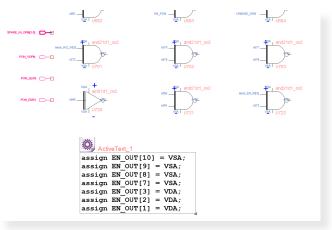
In the continuity of the reinforcement of the link between SLED and SMASH, SLED 2.3 notably improves the capability to add simulation directives directly in the schematic. Designers can integrate simulator control directives into top-level schematics, paving the way to the setup of the testbench and the configuration of all simulations directly from the schematic editor SLED.



Overview of SLED Schematic Editor

KEY FEATURES OF SLED 2.3

- Setting of simulation directives in schematics with active text boxes
- Enhanced Verilog import with the capability to display non structural code as active text
- Implemented capability to generate netlists directly from SLED API



Example of Verilog code displayed as active text after the import of a Verilog model

HIGH FLEXIBILITY AND CONFIGURABILITY WHEN SETTING SIMULATION DIRECTIVES IN THE SCHEMATIC

SLED 2.3

- Capability to hide/show and activate/deactivate text boxes
- Capability to select the design context and the modeling language for which each directive is active

Пор.и	
`timescale 1ns/10ps ^	
New Plander, in de aneigh 1 de san anna m	
`include "disciplines.vams"	
`include "constants.vams"	T
'include "switch.vams"	
module top (P,VP);	
inout VP;	
inout P;	
reg control;	
electrical VP;	
electrical P;	- /
ground electrical PowerSignal GND;	
🖯 initial begin	
control = 1'b0;	
<pre>forever #100 control = ~control;</pre>	
end	
resistor #(.res(10.0)) r0 (VP,P);	
<pre>vsine #(.ampl(1.0),.freq(1M)) v0 (VP,PowerSignal GND);</pre>	
switch sw0 (P, PowerSignal_GND, control);	
Lendmodule 🗸 🗸	
٢ >	
	-

Simulation directive added in the netlist file

include switch model	
<pre>register_control reg_control;</pre>	
active led instance switch witch sw0 (P, PowerSignal_GND, cor	SMACH Devolves transmet .Ifrace Tran Default top.control .Trace Tran V(P) V(VP) Min-1.1999997e+000 +Mar-1.1999976+000
adive_text_initial	.H 1fs 1fs 1ns 125m 2 .Tran 0s 5us 0s noise=no noisestep=lns traceBreak=ye + compress=no compressCoeff=l compressTolX=0 + compressTolY=lu powerup=no timeup=0s .Mathod BE lte=no
initial begin control = 1'b0;	

Example of simulation directives displayed in schematic

Property e	ditor			Property edito	r 📕
ActiveText				ActiveText	
SMASH_Dire	ctives			register_control	
Features		^ \$		Features	^ \$
Instance name:				Instance name:	
SMASH_Directives				register_control	
ActiveText		^ ¢		ActiveText	^ ¢
Properties:				Properties:	
Activate on top only	No			Activate on top only No	
Activate when flavour is	VERILOG		9	Activate when flavour is	VERILOG
Activate with configurations	Any			Activate with configurations Any	e
D' 1 1 1 1	Yes			Position in netlist post	t-module-ios
Display text on instance				A . A	
Include file name				Set after instance	

Property editor for active text

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