Missing EDA Links

SLED 1.7

DOLPHIN INTEGRATION

Productivity

Ergonomics

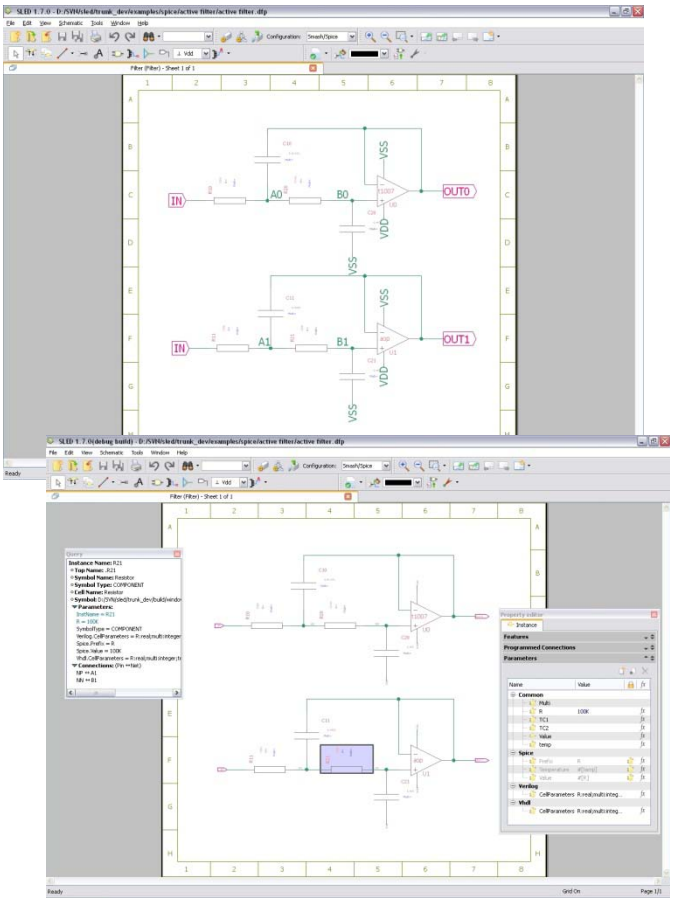
Design Checking

SLED 1.7 will satisfy the expectations of many designers as it includes significant user interface enhancements, as well as new features allowing to simplify the creation of advanced schematics with bus expressions, programmable pass-thru net connections... The verification of designs is significantly extended with custom design rules using the integrated Design Rule Checker.

SLED 1.7 increases designer productivity and enables automating design verification!

KEY ENHANCEMENTS AND FEATURES

- ✓ Enhanced net name definitions with bus expressions to increase design productivity and simplify repetitive schematics, such as transistor arrays
- ✓ Simplified wiring of pins and nets with automatic snapping to electrical objects, including off-grid objects
- ✓ Added the possibility to mark instances to be ignored during netlisting according to the target design context
- ✓ Implemented pass-thru net connections using programmed connections between pins of an instance
- ✓ Extended the Design Rule Checker with the capability to create user defined custom rules
- ✓ Extended hierarchical navigation using Push and Pop to HDL descriptions
- ✓ Improved the organization and configurability of the user interface to save screen space, remember the user setup and provide quick hiding of all floating or docked panels



DESCRIPTION OF THE IMPROVEMENTS

- Important progress has been made to improve the look and ergonomics of the integrated development environment provided by SLED. The toolbars have been refined by grouping similar icons (e.g. icons for designing geometrical shapes, zoom) and the tool panels are now dockable and movable. The area used for the schematic editor window can be optimized with a simple shortcut.
- When navigating through the hierarchy via push and pop, the designer can easily identify the active mode, edition or navigation, thanks to a color code. A single click allows to switch from one mode to the other.
- The .LSTB directive for linear loop stability analysis has been implemented in SMASH. On the schematics side, this directive requires conditional netlisting of a specific instance which is otherwise replaced by a pass-thru net connection with a programmed connection.

SLED is available identically under Linux and Windows.

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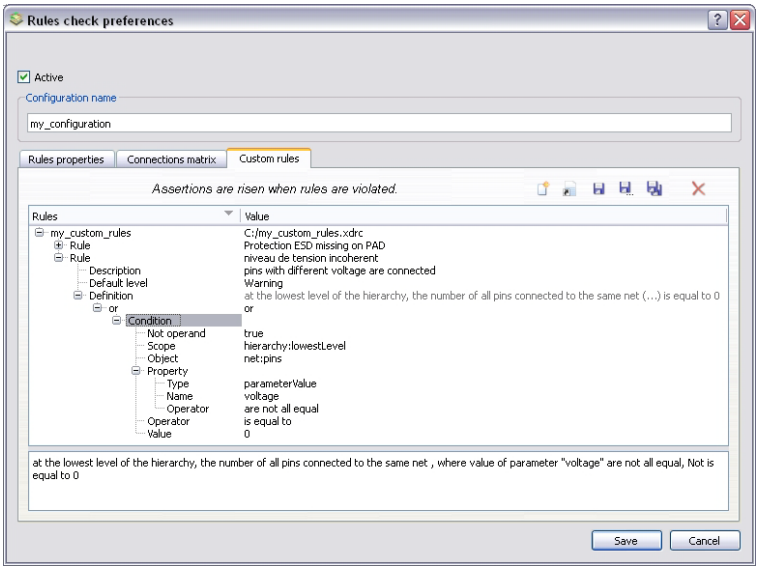
DOLPHIN INTEGRATION

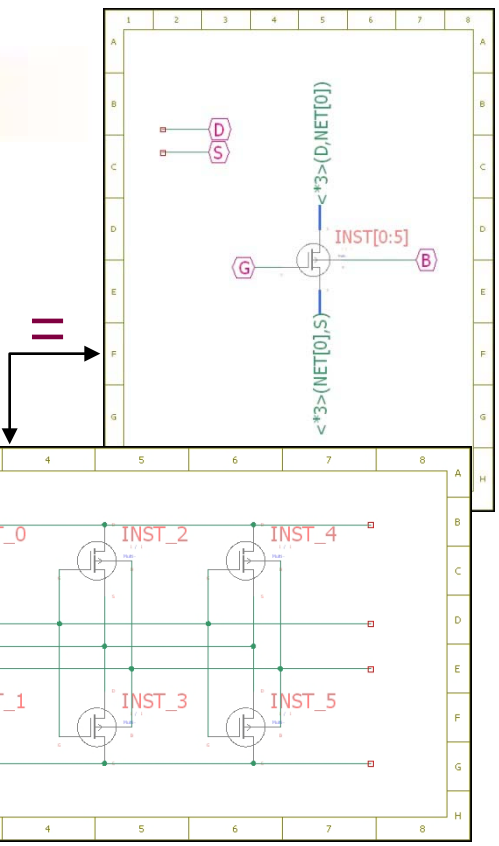
Custom Rule Checks & Bus Expressions



The Design Rule Checker has been available in SLED for one year. Customers now master the use of the default rules built-into SLED and have expressed the need to create their own rules for automating specific verifications, whether inherent to their design methodology or design related.

In SLED 1.7, designers can create and integrate custom rules through a graphic interface. The file defining the rules can then be shared with the design team or integrated into the design flow.

A component can often be instantiated several times in the same schematic. In order to avoid instantiating multiple symbols and drawing the nets to connect them with the rest of the design, designers have the possibility to use bus expressions. In this case, a symbol can be instantiated just once with an instance name the specifies the number of instances, and the input and output net names indicate how the connections are established.



A typical application for this feature is the creation of matrix such as a transistor array with serialization and parallelization.

Without bus expressions, the designer must perform a tedious matrix interconnection with no added value: see the screen shot...

Bus expressions allow designers to save valuable time and enable them to have more easily readable schematics!

HIGHLIGHT

Don't miss out discovering the new "**ICD - Interactive Curve Display**" solution for waveform viewing.

SLED is available identically under Linux and Windows.

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