EDA Presentation Sheet

SLED 1.5

DOLPHIN INTEGRATION

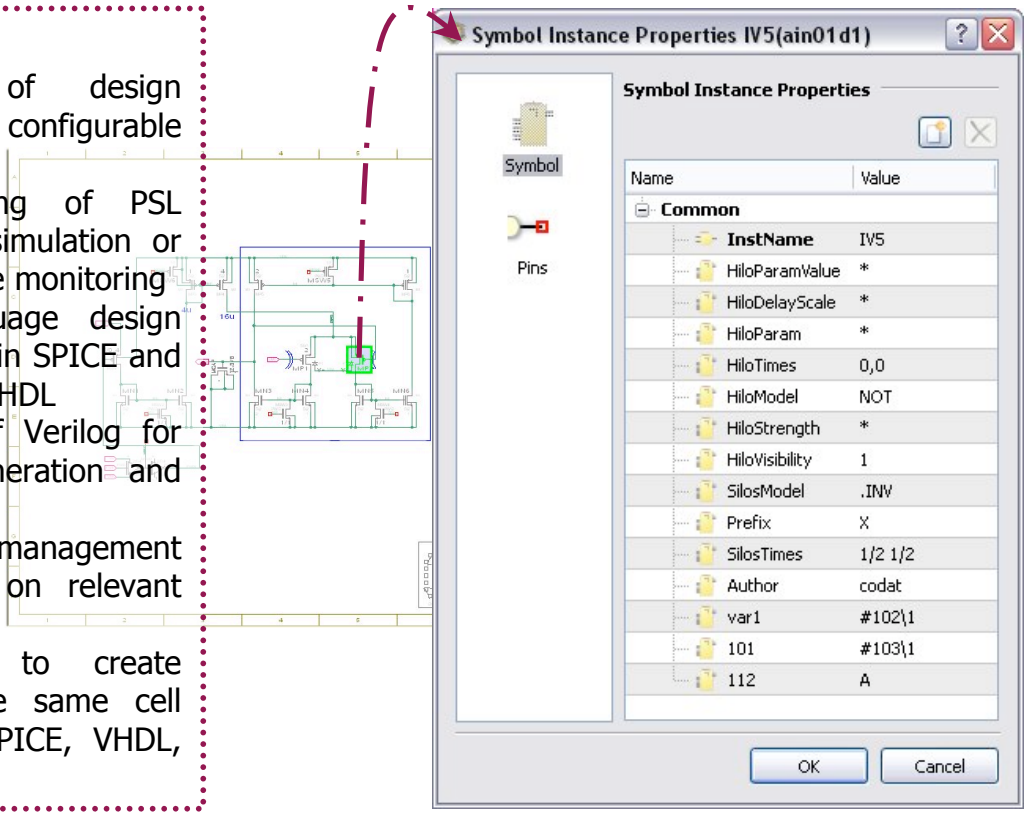
Hierarchical Design Rule Checker and PSL Assertions

Third generation Schematic Link Editor, SLED, helps increase designers' productivity with graphic link and configuration entry for plugging assertion-based checks and easing hierarchical verification. As verification takes most of designers' time, this release of SLED increases design robustness while decreasing verification time thanks to assertions in PSL (Property Specification Language) and efficient Design Rule Checks.

SLED 1.5 improves design robustness and enhances the design verification process!

KEY ENHANCEMENTS

- ✓ Quick localization of design problems through user configurable Design Rule Checker
- ✓ Schematic link editing of PSL verification units for simulation or for embedded hardware monitoring
- ✓ Enhanced mixed-language design using blocks described in SPICE and Verilog, in addition to VHDL
- ✓ Integrated handling of Verilog for automatic symbol generation and netlisting
- ✓ Streamlined property management with display focused on relevant properties
- ✓ Extended possibility to create several views for the same cell (symbol, schematic, SPICE, VHDL, Verilog…)



DESCRIPTION OF THE BENEFITS

The bundle SLASH of SLED and SMASH natively supports the synthesis and simulation of PSL assertions. Logic designers can graphically link PSL assertions* of the expected behavior into the design. These can then be simulated jointly in SMASH to detect bugs earlier, or to locate faster the causes of problems.
Furthermore, the SLED-SDG option provides the means to generate synthesizable hardware checkers in Verilog or VHDL from PSL assertions. These checkers can then be embedded into an FPGA, a testchip, a secure circuit or a mission critical circuit for monitoring purposes. The generated hardware monitors can be used in any design flow.

For increased designer productivity, SLED delivers enhanced property management enabling to add selectively properties to libraries, cells, symbols and instances. The values of properties can be propagated and the user can define on which objects the value of a property is editable. Mandatory properties can be defined with no default value: values are then required on the instance. Libraries, cells, symbols and instances contain and display relevant properties only.

*TIMA technology under UJF/Grenoble INP license

SLED is available identically under Linux and Windows.

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DOLPHIN INTEGRATION

Improve verification time at the design stage with the Design Rule Checker

Designers fed up with long verification time and tired of discovering design problems at the end of the design flow, or worse after fabrication, will appreciate the new Design Rule Checker delivered in SLED.

In only 3 simple steps, it is possible to configure the rule checker, locate potential problems and correct them!

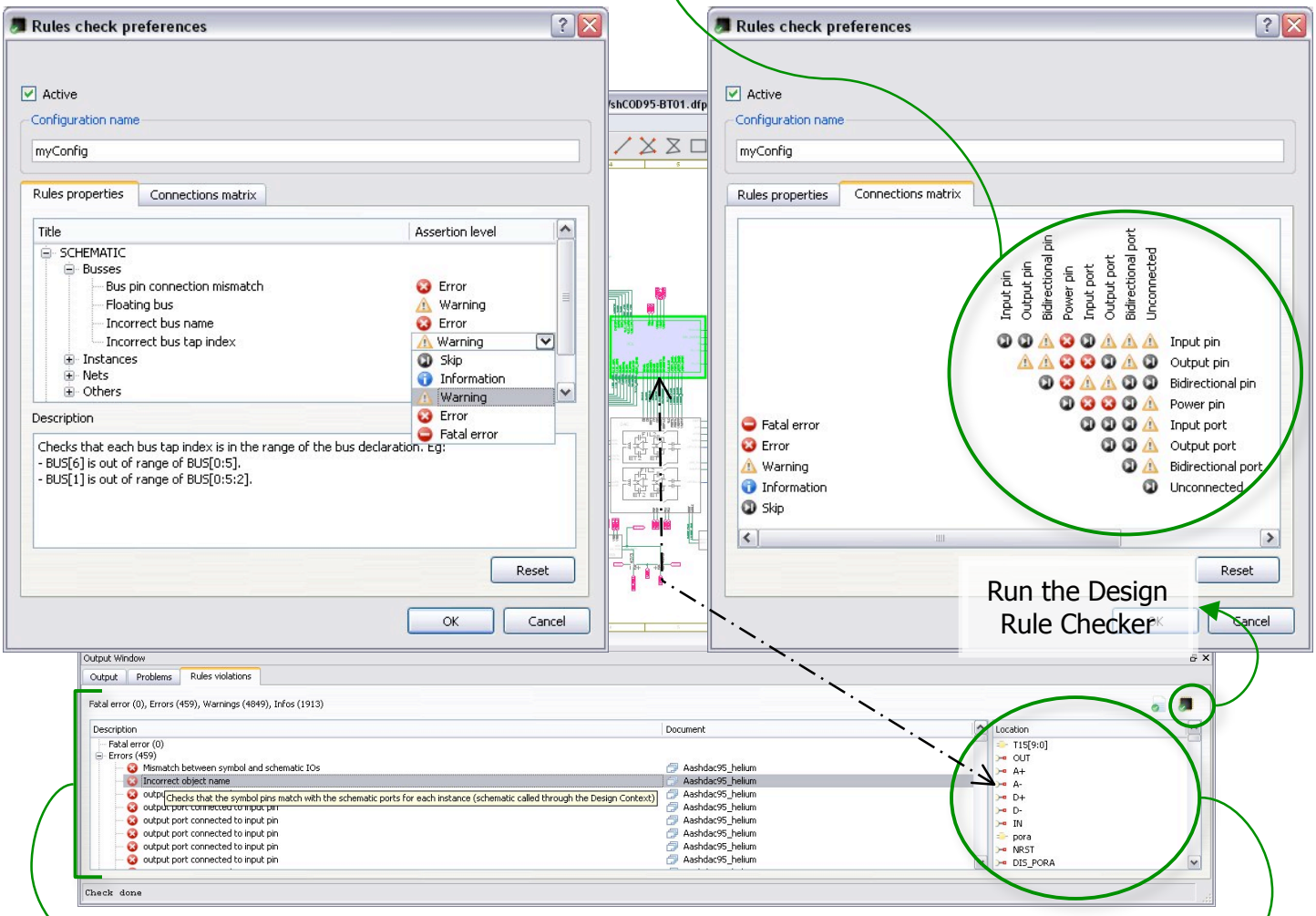
Visualize the connections defined between pins and ports or pins between them and change them with only two clicks

Step 1

Select the relevant assertion level for each rule

Step 2

Decide what should be the connection rules



Step 3

Run the Design Rule Checker and correct the problems highlighted in the report

Automatic classification of rule violations

Easy localization of the problem by clicking on the element names

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