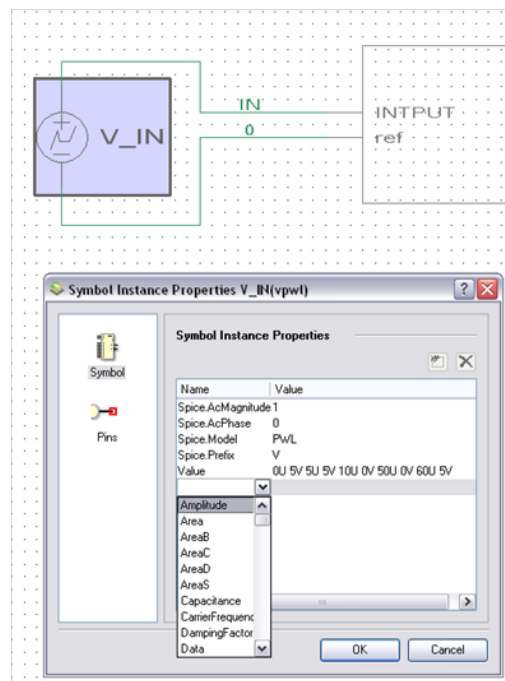


Schematics Edition had lost its luster for lack of innovation which resulted in the perception that Hardware Description Languages had made it obsolete. But the essence of any conceptualization can only be graphical: any designer thinks in images, not in words. Beyond the traditional bottom-up practice of interconnecting analog or logic primitives, in view of the top-down techniques needed for mixed signal and multi-domain designs, **SLED 1.2** paves the road to the Schematics Editor of the third generation embedding the Link-Edit capability of Hardware Description Languages.

KEY ENHANCEMENTS

- ✓ Simplified manipulation of schematics by dragging symbols while preserving wire connections
- ✓ Dynamic link with SMASH for cross-probing from schematics to waveform results
- ✓ Enhanced netlist generation for multi-flavor SPICE support (device sorting, line length limits...)
- ✓ Streamlined graphic configuration of application preferences (grid and cursor, colors, access codes, constants, default properties of symbols, pins...)
- ✓ Easy graphic edition of library properties including handling of library constants for property values
- ✓ Enhanced graphic edition of cell properties including constants for property values
- ✓ Simple graphic edition of symbol and pin properties



DESCRIPTION OF THE ENHANCEMENTS

SLED 1.2 enables the intimate linking with the DOLPHIN SMASH Simulator: this new bundle becomes a reference for mixed-signal, multi-level or multi-domain simulation. Users can drive their design investigation and curve display from their schematic capture...

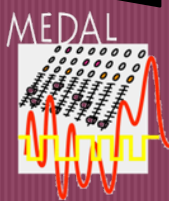
The enhanced property support adds a new dimension to schematic edition. Parameter assignment to symbols, independently of the modeling language, avoids language specific syntax errors, and enables configurable multi-language netlisting. Visual modeling and link-editing enable management of constraints and directives from the beginning of the design through the layout, simulation, DRC or LVS applications.

Furthermore, multi-domain designers are guided during wiring of symbols with intelligent type checking of terminals. Early stage messages inform the designer during link-editing of schematics about misconnections, and not only at the later netlisting stage, to avoid time consuming investigations.

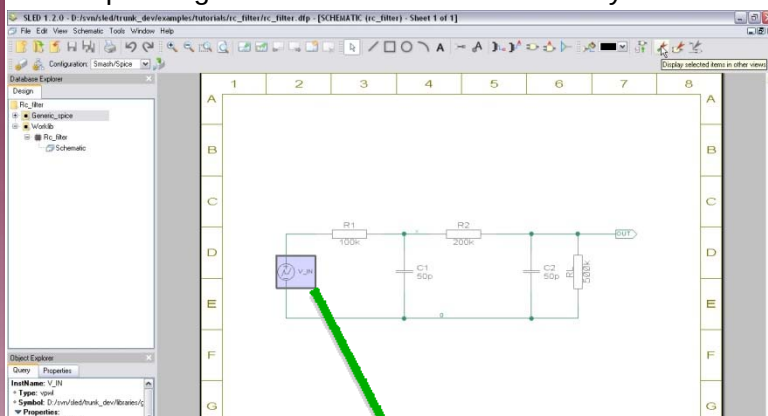
Schematics capture finally becomes the central element of your flow!



SLED is available identically under Linux, Solaris and Windows.

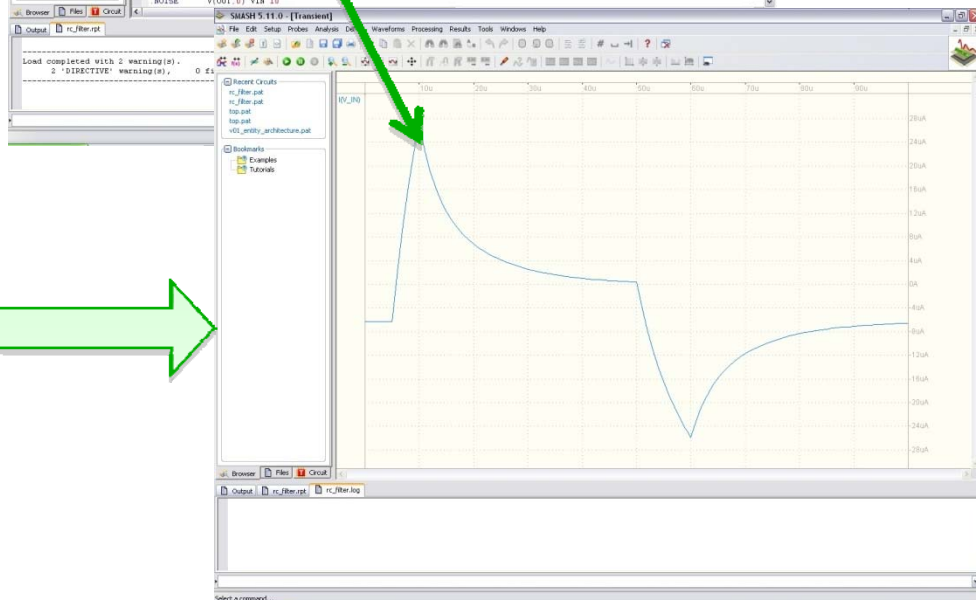


Bundling SLED and SMASH enables straightforward graphic integration from entry to waveforms: netlists are automatically loaded in SMASH after generation from the schematics editor. Dynamic cross-probing becomes feasible, even when a simulation is running. For instance, with a single click, cross-probing will display the waveforms in SMASH corresponding to the nets or devices currently selected in the schematics.



Select a net or device in SLED
Activate the cross-probe command from the toolbar
View the waveform in SMASH

Output Log Debug
Netlist (SPICE) rc_filter
D:\dev\slashed\trunk\dev\examples\tutorials\rc_filter
D:\dev\slashed\trunk\dev\examples\tutorials\rc_filter
D:\dev\slashed\trunk\dev\examples\tutorials\rc_filter
Trying to connect to Smash simulator - cfigi
Smash simulator - cfigi: Server connected
Smash simulator - cfigi: Circuit is loaded
Display selected items in other views



SLASH is available identically under Linux, Solaris and Windows.