

SLED 1.1 Schematics Link Editor



Schematics Edition had lost its luster for lack of innovation which resulted in the perception that Hardware Description Languages had made it obsolete. But the essence of any conceptualization can only be graphical: any designer thinks in images, not in words.

Beyond the traditional bottom-up practice of interconnecting analog or logic primitives, in view of the top-down techniques needed for mixed signal and multi-domain designs, **SLED 1.1** performs the transition to the Schematics Editor of the third generation embedding the Link-Edit capability of Hardware Description Languages.

KEY ENHANCEMENTS

- ✓ Increased ergonomics with productivity enhancing user interface improvements
- Extended attribute values with global variables and function calculated values
- ✓ Extended compatibility with ECS symbol and schematic ASCII files (properties, net attributes...)
- ✓ Generic library of SPICE components for direct use in analog schematics
- ✓ Built-in handling of Design Context configurations for multi-flavor SPICE netlisting (SMASH, Hspice, SDL, LVS...)
- ✓ Improved cell tree viewing of VHDL and VHDL-AMS entities and architectures with direct access to model source code
- ✓ Graphic VHDL/VHDL-AMS link editing and netlisting for system level modeling



DESCRIPTION OF THE ENHANCEMENTS

For design of analog circuits, the generic library of SPICE components, combined with multiflavor SPICE netlisting, improves designers' productivity by enabling the creation of true mixed signal circuits, as state-of-the-art analog designs including hand-crafted logic. The configuration of Design Contexts enables netlisting with the appropriate SPICE flavor respectively for analog simulation, for Schematic Driven Layout (SDL) and for Layout Versus Schematic (LVS) without requiring any change to the schematics.

For design of multi-domain systems, typically for Micro Electro Mechanical Systems (MEMS) where the mechanical structure is best represented in VHDL-AMS, the capability was missing for a graphic entry of elementary models to create a complex dynamical model by graphic composition. Homogeneous netlisting is a must for performing fundamental spectral analysis of the whole MEMS, as both the designer of Analog Circuit and the designer of Mechanical Structure are used to practicing separately.



🧱 SLED is available identically under Linux, Solaris and Windows.

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Accelerometer device testbench

SLED 1.1 VHDL-AMS Link Editing

Enriched with the EMBLEM-Mecha library of basic effects and connected to the multi-domain simulator SMASH, **SLED provides the ideal MEMS modeling platform for the design of multi-domain systems.**

Hierarchical push into the structure of the accelerometer device.

Comb drive

Sled Release

KEY FEATURES

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✓ Graphic VHDL/VHDL-AMS link editing for modeling of MEMS and multi-domain systems

Sled Release:

- Easy push/pop navigation through hierarchical schematics with multiple wire highlighting
- ✓ Access to VHDL and VHDL-AMS model source code of entities/architectures from cell tree view
- ✓ Configurable cell pin attributes for signal types and terminal natures
- ✓ Interactive propagation of types and natures to wire connections between pins
- ✓ Hierarchical configuration of instance architectures for netlisting
- ✓ Direct netlisting to VHDL/VHDL-AMS with integrated terminal type checking

Hierarchical push into the comb drive.

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VHDL-AMS source code of beam

DESCRIPTION OF THE EASE OF USE

SLED delivers the intuitive graphic entry, which designers already master for circuit design, for electro-mechanical devices and systems. Dealing with mechatronic system or MEMS design becomes as simple as graphically interconnecting blocks to create multi-domain systems including electronics and mechanics.

Simply click'n drop symbols of any blocks from generic or adhoc libraries to assemble your design, be it a device or a circuit. Model parameters are directly accessible in the properties pane on the right. Working with different domains is fail proof as SLED automatically checks the connections between terminals by comparing their types and issues warnings when invalid connections are wired.



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MEDAL Presentation Sheet