# Missing EDA Links

## SLED SDG

DOLPHIN INTEGRATION

PRELIMINARY

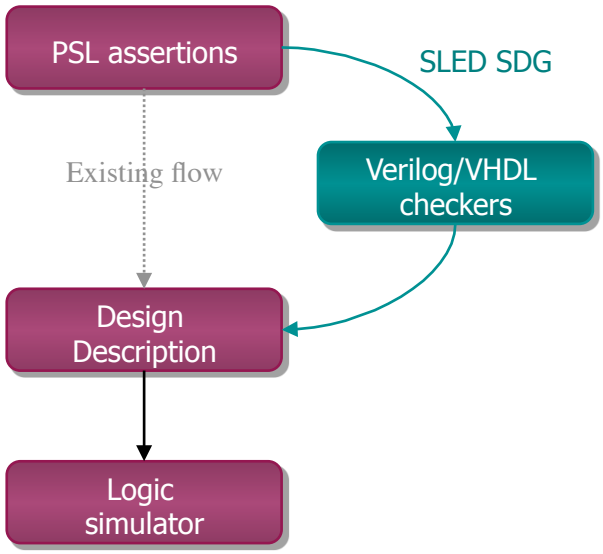
## The solution for bug trappers

As design verification takes up to 70 % of the overall design time, the most important productivity gains are reached by reducing time needed for verification while increasing verification coverage. Assertion-Based Verification (ABV) enables ensuring that the behavior of a design meets its specification from its earliest stage onward.

**SLED SDG** (Synthesizable Detector Generator) is dedicated to improving productivity when using assertions by providing automatic generation of RTL checkers (Verilog or VHDL) from PSL (Property Specification Language) assertions. **Such checkers can be used both for virtual test and in-circuit embedded test!**

### KEY BENEFITS of SLED SDG

- ✓ Point-solution to convert smoothly PSL properties into synthesizable Verilog/VHDL modules
  - ⇨ Assertion checkers help verify the behavior of the circuit
  - ⇨ Assumption injectors generate property-based random test patterns
- ✓ Acceleration of the simulation of assertions
  - ⇨ Benefit from simulator specific RTL simulation optimizations
- ✓ Replacement of PSL assertions in design descriptions with optimized RTL implementations
  - ⇨ Identical assertions before and after synthesis
- ✓ Accessible through shell command line
  - ⇨ Easy integration into design flows using scripts
- ✓ Integration of RTL synthesizable hardware checkers into circuits for real-time verification
- ✓ Selectable and customizable control and event collector interfaces for easy hardware integration




### ASSERTION-BASED VERIFICATION (ABV)

Today, assertions are an integral part of the design and verification process and are becoming more and more popular. In much fewer lines of code than corresponding VHDL or Verilog descriptions, assertions facilitate and automate the verification process by helping detect hard to find bugs through analysis of simulation results.

Digital designers are faced with the need to simulate huge circuit descriptions while leveraging non-regression test and verification techniques. As the support of PSL may not be optimized in usual logic simulators, converting PSL assertions into Verilog or VHDL with SLED SDG allows to reduce simulation time in the digital simulator of choice by benefiting from the simulator specific RTL simulation optimizations while maintaining the benefits of assertions.

As the use of assertions is not restricted to virtual test, the RTL checkers generated by SLED SDG can be synthesized and embedded into FPGA, testchip and even on-chip to monitor events and violations which can appear under real conditions.

*TIMA technology under UJF/Grenoble INP license

**SLED is available identically under Linux and Windows.**

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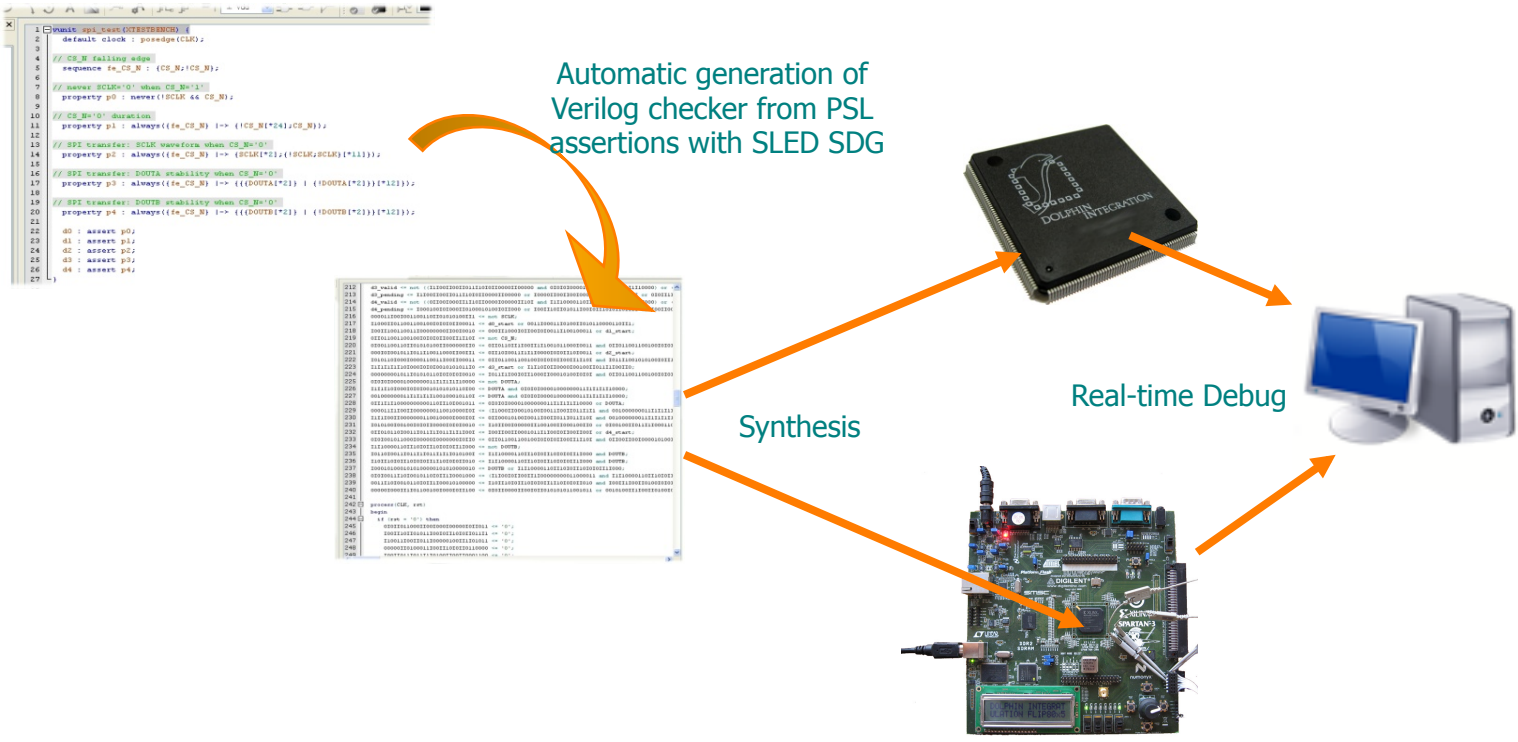
## Securing a design with embedded assertions

SLED SDG extends Assertion-Based Verification (ABV) to the hardware world thanks to the conversion of PSL assertions into Verilog/VHDL checkers. These checkers can then be synthesized for:

- assessing a chip or FPGA in real conditions
- being sure of the reliability of a secure circuit or a mission-critical circuit all along its lifespan thanks to self-test and automatic diagnosis assistance

When using assertions in simulation, detected events and violations are generally reported to the designer in the simulator log file which can be post-processed manually or automatically to analyze the information reported. When using assertions embedded in hardware, events and violations must be collected and reported to the designer through tradition means, such as µcontroller / µprocessor interfaces, serial JTAG interfaces… in order to be as less invasive as possible.

The selectable and customizable control and event collector interfaces proposed by SLED SDG integrate with traditional debug infrastructures, centralize the signals coming from the checkers and enable easy hardware integration.




**Typical cases where embedding hardware checkers is helpful**

- For testchips and FPGA: to benefit from real-time execution of the circuit for comprehensive monitoring and to correlate behavior observed in simulation and during physical test.
- For mission critical SoCs: even if assertions are not triggered during the verification process, they might be violated later during the exploitation phase of the circuit. When the SoC targets security or critical applications, the checkers can send signals or alerts when specific events, errors or unexpected conditions occur, and corrective actions can be put in place as fast as possible.

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