DOLPHIN DESIGN

New Features

SLED 3.6.0

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Contents

THANKS

As always for new releases, we would like to thank those customers who take the time to report problems and/or to suggest improvements (please remember that the best way to do so is by sending an email to support@dolphin.fr or contact@dolphin.fr with an accurate description of your problem or suggestion, together with the relevant files if any). As you will see in the new features, we do our best to take remarks into account. And even if your suggestion does not appear this time, don't think it was lost or disregarded. Simply, it means that its implementation could not fit into the development plan for this particular release, but be assured that we will try to take it into account in a future release.

WEB SITE

Our web site www.dolphin-design.fr is a source of information on our EDA solutions. Aside from evaluation kits for our products, a number of application notes, courses or upgrades are available for download.

SLED

SLED is a hierarchical schematic entry solution of the third generation which delivers the long awaited dual capability for Graphic Entry and Scriptability at once. It blends efficiently the feasibility of linking components and of writing scripts for configuring a netlist hierarchically. Interoperability with other schematic entry tools is ensured for capitalizing on legacy designs and cooperative work, and interoperability in the Design Chains is ensured through standard design exchange formats and scriptability for customization by CAD managers.

PSL

Relevant options of SMASH include native support for simulation of PSL[1] properties, both assertions and coverage, with very low time and memory overhead.

The integration of PSL is complete with source code syntax coloring, association of verification units with Verilog or VHDL models or instances, logging of PSL assertion violations, reporting of PSL sequence coverage results, and breaking into the source level debugger for investigation of design defects.

Assertion-Based Verification

The SLED SDG[2] option enables conversion of PSL assertions into synthesizable RTL models. This makes it possible for the designer to automatically integrate PSL verification units into a Design Under Test in an FPGA for emulation or in a testchip. Embedding hardware verification units in prototypes increases verification speed by several orders of magnitude.

Automated generation of synthesizable models from PSL assertions can also be used as an efficient alternative to writing safety related parts of a design directly in RTL. These hardware verification units are integrated for embedded monitoring.

[1] Property Specification Language
[2] Synthesizable Detector Generator

SUPPORTED PLATFORMS

Microsoft Windows

SLED is designed to run on Microsoft Windows Vista / 7 / 8 / 10 on x86_64 platforms.

Linux on Intel x64 platform

SLED is designed to run under X-Window on RedHat Enterprise Linux 6 (RHEL6) and supports compatible Linux distributions on x86_64 platforms.

CREDITS & COPYRIGHTS

Qt : A C++ framework for cross-platform programming

http://qt.digia.com

Qt Development Frameworks creates application development platforms for desktop and mobile device innovation.

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LIBJSON Component

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SLED

SLED

Bug fixing

- Corrected the display of image in the symbol view (DDIsa13977 - SLED 3.6.0)