

DOLPHIN

DESIGN

New Features

SLED 3.5.2

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Dolphin Design SAS

1bisA Chemin du Pré Carré - 38240-MEYLAN - FRANCE

Phone: + 33 476 411 096 - Fax: + 33 476 902 965

www.dolphin-design.fr - contact@dolphin.fr

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THANKS

As always for new releases, we would like to thank those customers who take the time to report problems and/or to suggest improvements (please remember that the best way to do so is by sending an email to support@dolphin.fr or contact@dolphin.fr with an accurate description of your problem or suggestion, together with the relevant files if any). As you will see in the new features, we do our best to take remarks into account. And even if your suggestion does not appear this time, don't think it was lost or disregarded. Simply, it means that its implementation could not fit into the development plan for this particular release, but be assured that we will try to take it into account in a future release.

WEB SITE

Our web site www.dolphin-design.fr is a source of information on our EDA solutions. Aside from evaluation kits for our products, a number of application notes, courses or upgrades are available for download.

SLED

SLED is a hierarchical schematic entry solution of the third generation which delivers the long awaited dual capability for Graphic Entry and Scriptability at once. It blends efficiently the feasibility of linking components and of writing scripts for configuring a netlist hierarchically. Interoperability with other schematic entry tools is ensured for capitalizing on legacy designs and cooperative work, and interoperability in the Design Chains is ensured through standard design exchange formats and scriptability for customization by CAD managers.

PSL

Relevant options of SMASH include native support for simulation of PSL¹ properties, both assertions and coverage, with very low time and memory overhead.

The integration of PSL is complete with source code syntax coloring, association of verification units with Verilog or VHDL models or instances, logging of PSL assertion violations, reporting of PSL sequence coverage results, and breaking into the source level debugger for investigation of design defects.

Assertion-Based Verification

The SLED SDG² option enables conversion of PSL assertions into synthesizable RTL models. This makes it possible for the designer to automatically integrate PSL verification units into a Design Under Test in an FPGA for emulation or in a testchip. Embedding hardware verification units in prototypes increases verification speed by several orders of magnitude.

Automated generation of synthesizable models from PSL assertions can also be used as an efficient alternative to writing safety related parts of a design directly in RTL. These hardware verification units are integrated for embedded monitoring.

¹Property Specification Language

²Synthesizable Detector Generator

SUPPORTED PLATFORMS

Microsoft Windows

SLED is designed to run on Microsoft Windows Vista / 7 / 8 / 10 on x86_64 platforms.

Linux on Intel x64 platform

SLED is designed to run under X-Window on RedHat Enterprise Linux 6 (RHEL6) and supports compatible Linux distributions on x86_64 platforms.

CREDITS & COPYRIGHTS

Qt : A C++ framework for cross-platform programming

<http://qt.digia.com>

Qt Development Frameworks creates application development platforms for desktop and mobile device innovation.

Qt Development Frameworks Oyj, Valimotie 21, 00380 Helsinki Finland +358 10 313 3000 © 2012 Digia. Legal and Privacy

Scintilla Source Code Editor Component

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LIBJSON Component

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SLED

SLED

Enhancements

- Implemented the ability to use a prefix for the labels name in an instance decoration (DDIsa12156 - SLED 3.5.0)
- Implemented the support of TCL procedures evaluation in Tag description (DDIsa13699 - SLED 3.5.0)
- Implemented means to open an UPF file with syntax highlighting from an URL in an HTML page (DDIsa13712 - SLED 3.5.0)
- Improved the visibility of the Project Manager items tooltip (DDIsa13781 - SLED 3.5.0)
- Implemented the ability to rename a hierarchical object from its contextual menu item (DDIsa07296 - SLED 3.5.1)
- Implemented means to show/hide instance pin in schematic (DDIsa13647 - SLED 3.5.1)
- Implemented means to define tags attributes in cell parameter definition (DDIsa13795 - SLED 3.5.1)
- Implemented the management of the read-only attribute of parameter defined in a cell by a tcl procedure (DDIsa13797 - SLED 3.5.1)
- Implemented the ability to set a color driven by a tcl script (DDIsa13816 - SLED 3.5.1)
- Implemented automatic ascent of hierarchicat parameters #(xx) from schematic instances to cell (DDIsa13826 - SLED 3.5.1)
- Implemented the support of error status in return of TCL procedures called when evaluating the value of the parameters (DDIsa13855 - SLED 3.5.1)
- Implemented the ability to create of a new work library just after creating a project (DDIsa13959 - SLED 3.5.1)

Bug fixing

- Corrected the incorrect naming process when connecting a propagated instance pin on an unnamed net (DDIsa13568 - SLED 3.5.0)
- Corrected the ability to rename a cell of a locked library (DDIsa13592 - SLED 3.5.0)
- Corrected the display of parameters tooltip when it has to be evaluated (DDIsa13595 - SLED 3.5.0)
- Corrected the actions on locked schematic and symbol (DDIsa13599 - SLED 3.5.0)

- Corrected the unexpected adding of parameters in the new cell reference of an instance when the cell is locked (DDIsa13622 - SLED 3.5.0)
- Corrected the ability to rename a document of a locked library (DDIsa13633 - SLED 3.5.0)
- Corrected the Mark Net availability on locked schematic (DDIsa13641 - SLED 3.5.0)
- Corrected the resizing of the parameters pane columns when the selection changed (DDIsa13674 - SLED 3.5.0)
- Corrected the management of propagated pin after removing subnet connected to propagated instance pins (DDIsa13689 - SLED 3.5.0)
- Corrected the management of variable name case when several projects are loaded consecutively (DDIsa13744 - SLED 3.5.0)
- Corrected the Zoom Tool availability on locked schematics and symbols (DDIsa13766 - SLED 3.5.0)
- Corrected the instance connectivity corruption after changing the cell reference with a cell which has more pins than the initial one (DDIsa13773 - SLED 3.5.0)
- Corrected the loss of the wire style after renaming the net (DDIsa13784 - SLED 3.5.0)
- Corrected the unexpected opening of a new schematic editor after clicking on an instance link (DDIsa13783 - SLED 3.5.1)
- Corrected the rendering of the sheet decoration that may be erratic (DDIsa13796 - SLED 3.5.1)
- Corrected the edition of the Active Text on locked schematic (DDIsa13800 - SLED 3.5.1)
- Corrected the behavior of the Property Editor radius field of a multiple selection of arcs (DDIsa13801 - SLED 3.5.1)
- Corrected the ability to add the 'InstName' and 'CellName' property in a symbol view by using the 'Add Property Text' dialog (DDIsa13802 - SLED 3.5.1)
- Corrected the closing phase to always ask for saving modified views (DDIsa13803 - SLED 3.5.1)
- Corrected the management of application display after reducing the number of screens (DDIsa13825 - SLED 3.5.1)
- Corrected the parameter highlighting in the PEF after using its link (DDIsa13845 - SLED 3.5.1)
- Corrected the ability to copy a selection on a sheet of a locked library (DDIsa13846 - SLED 3.5.1)
- Corrected the content of the Hierarchical Configuration after duplicating cells or instances (DDIsa13863 - SLED 3.5.1)
- Corrected the application crash when displaying a schematic with its backannotation data and deleting the cell the schematic belongs to (DDIsa13894 - SLED 3.5.1)

- Corrected the saving of the variables during the preferences change (DDIsa13930 - SLED 3.5.1)
- Corrected the location of the netlisted circuit item in the 'Project manager' when a schematic with the same name has been netlisted previously (DDIsa13950 - SLED 3.5.2)
- Corrected the origin of the transformation after resizing a sheet object (DDIsa13976 - SLED 3.5.2)
- Corrected the evaluation of variable in parameter value when the parameter is related to an instance in the hierarchy (DDIsa13983 - SLED 3.5.2)

SLED API

Enhancements

- Implemented the ability to decorate a symbol instance from the API (DDIsa08986 - SLED 3.5.0)

Bug fixing

- Corrected the library type value in new API ("ref", "work" instead of 0, 1) (DDIsa13700 - SLED 3.5.0)

SLED DRC

Bug fixing

- Corrected the inconsistent result of the hierarchical DRC for graphic symbol instance (DDIsa13882 - SLED 3.5.1)
- Corrected the unexpected risen of the 'unconnected input pin' violation of the rule when a bussed pin is connected to a set of scalar ports (DDIsa13921 - SLED 3.5.1)
- Corrected the status of the checker buttons available in the 'Rules violation' window during the checker process (DDIsa13961 - SLED 3.5.2)

SLED NETLISTER

Enhancements

- Implemented the management in the parameter evaluation process of the ternary operator (condition)?a:b with strings operands in the condition (DDIsa13924 - SLED 3.5.1)

Bug fixing

- Corrected the instance url set as argument for the TCL procedure related to the onInstanceNetlisted hook (DDIsa13933 - SLED 3.5.1)